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Newgate

Schematics Document

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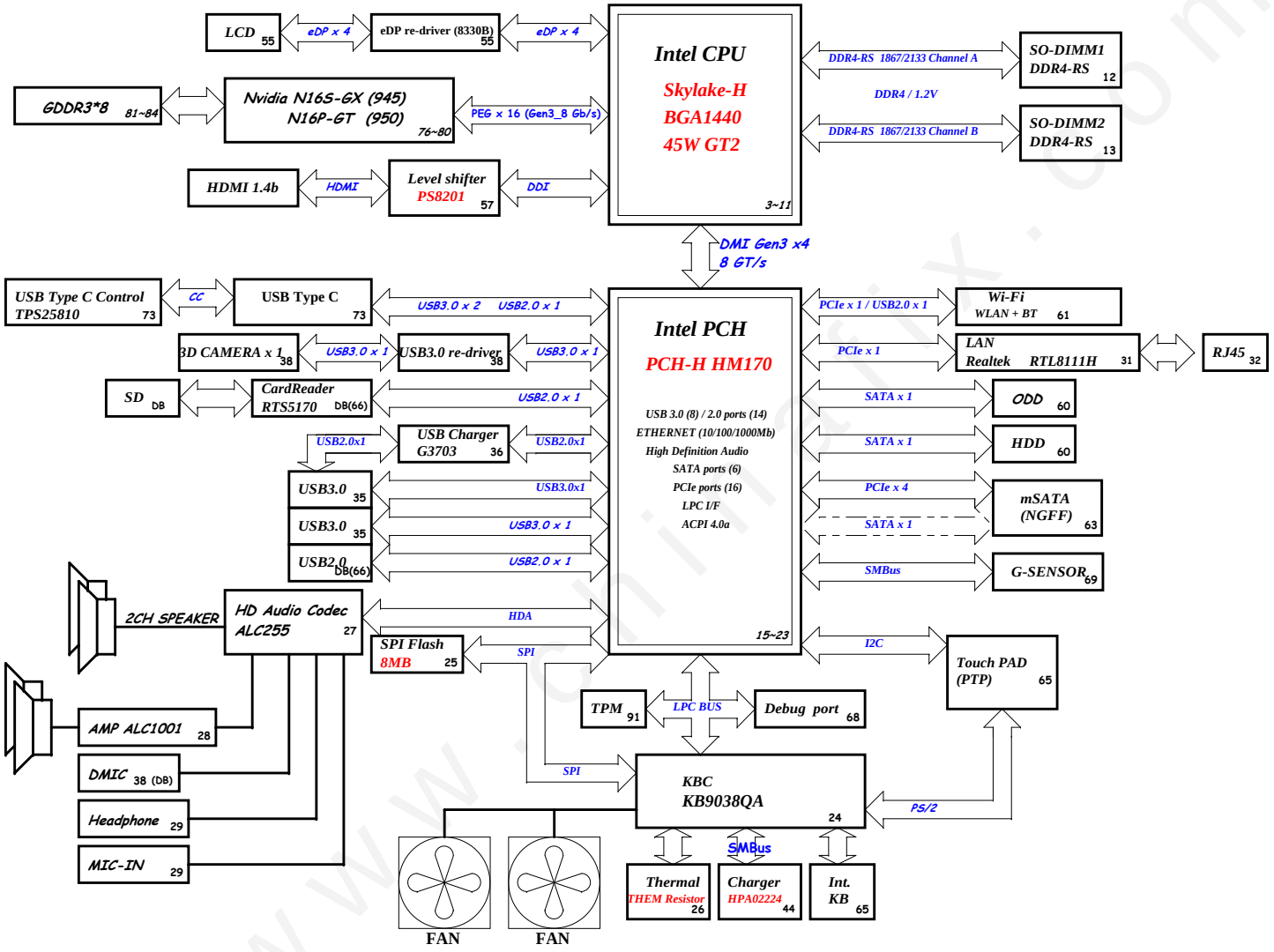
Title: **Cover Page**		
Size: A	Document Number: **Newgate**	Rev: **1M**
Date: Wednesday, August 12, 2015	Sheet 1 of 105	

Newgate Board Block Diagram

Project code : 4PD06A010001
PCB NO : 15205
Revision : 1M



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Title: Block Diagram

Size: C | Document Number: Newgate | Rev: 1M

Date: Wednesday, August 12, 2015 | Sheet 2 of 105

SSID = CPU

Royee 20150205 REVERSE PEG BUS for layout issue

HDMI

LAB2 0401 change

Layout Note:
Trace Width:12 (mils)
Spacing: 20 (mils)
Max Length: 100 (mils)

Layout Note:
Trace Width:12 (mils)
Spacing: 15 (mils)
Max Length: 400 (mils)

PD 0622 change

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Title: CPU (PCIE/DMI/FDI)

Size: Custom | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 3 of 105

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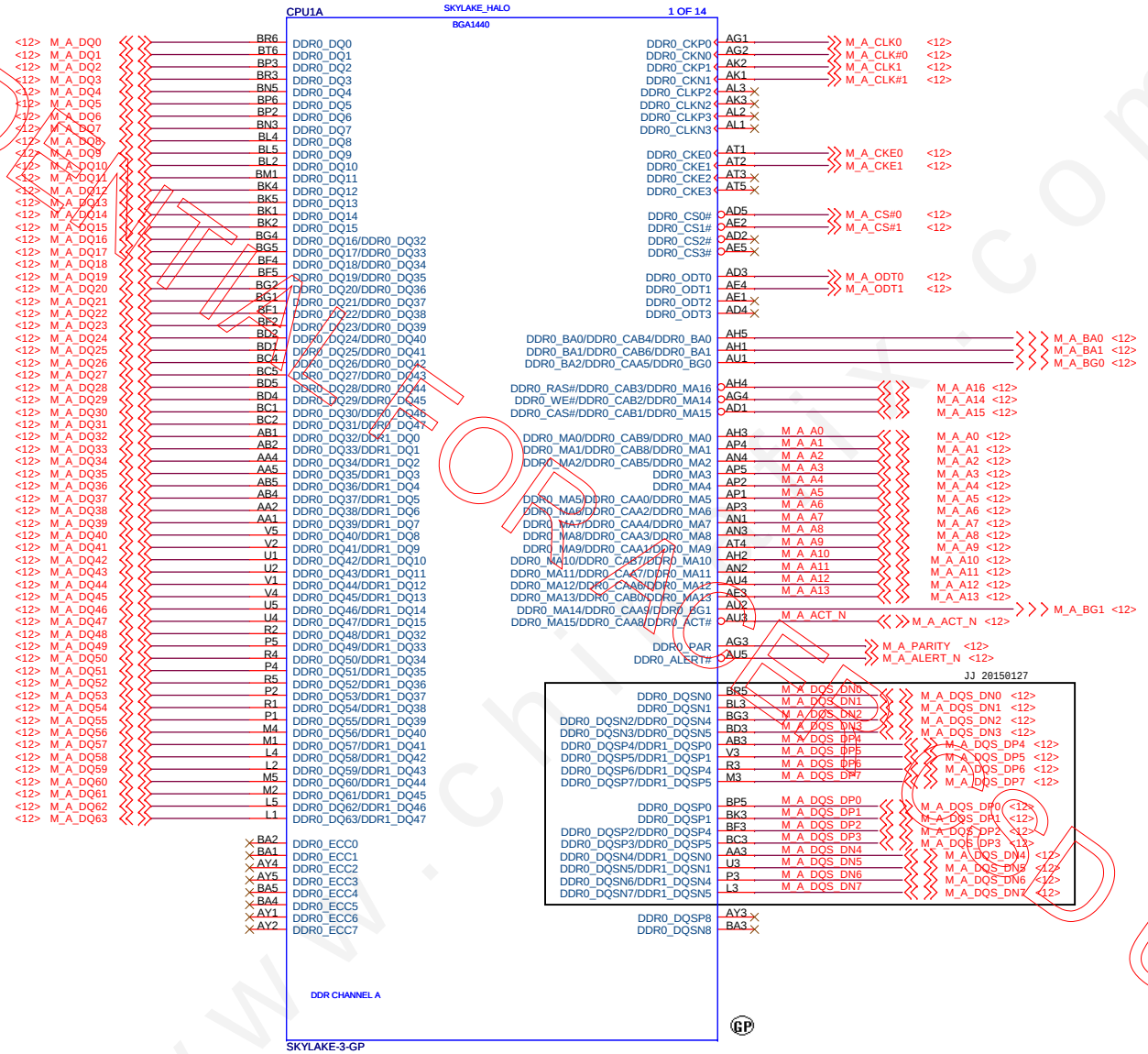

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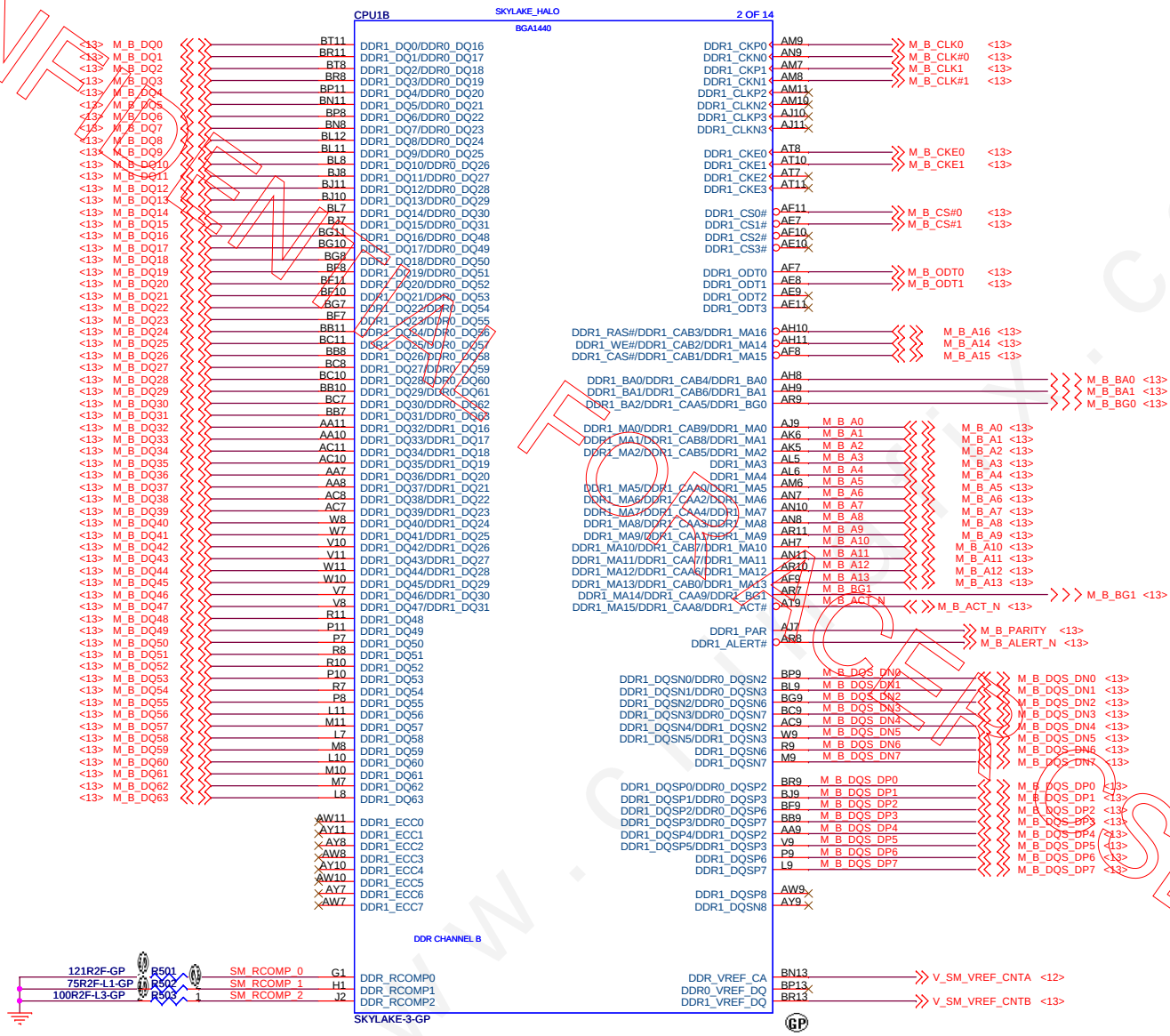
Title	CPU_DDR_CHA	
Size A3	Document Number Newgate	Rev 1M
Date: Thursday, August 13, 2015	Sheet 4 of 105	

SSID = CPU



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Title: CPU_DDR_CHB

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 5 of 105

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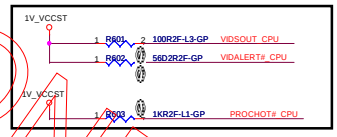
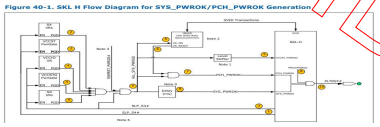
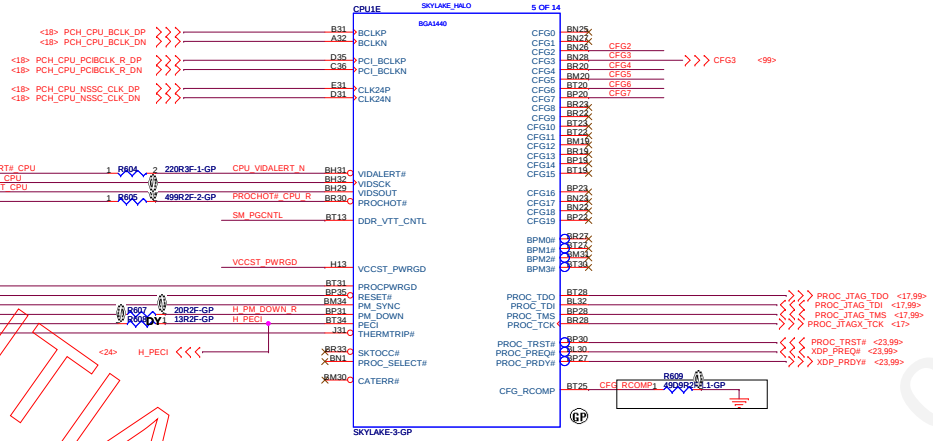
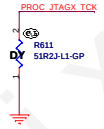
SSID = CPU

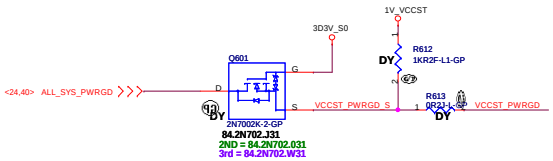
AROUND_CPU











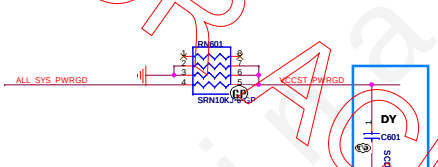


Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: – 1 = (Default) Normal Operation; No stall. – 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – 1 = Normal operation – 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: – 1 = Disabled. – 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation – 00 = 1 x8, 2 x4 PCI Express* – 01 = reserved – 10 = 2 x8 PCI Express* – 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: – 1 = (default) PEG Train immediately following RESET# de assertion. – 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

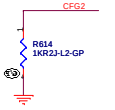
Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

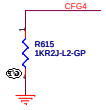
Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	Vcc_{IO}	16-60 Ω
PREQ#	Pull Up	Vcc_{ST}	3 kΩ
PROC_TDI	Pull Up	Vcc_{STG}[1]	3 kΩ
PROC_TMS	Pull Up	Vcc_{SGT}[1]	3 kΩ
CFG[19:0]	Pull Up	Vcc_{IO}	3 kΩ

Note:
1. For SKL-S it should be Vcc_{ST}

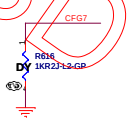
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



eDP Enable	
CFG4	1:Disable 0:Enable



PEG Training	
CFG7	1:(default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.



PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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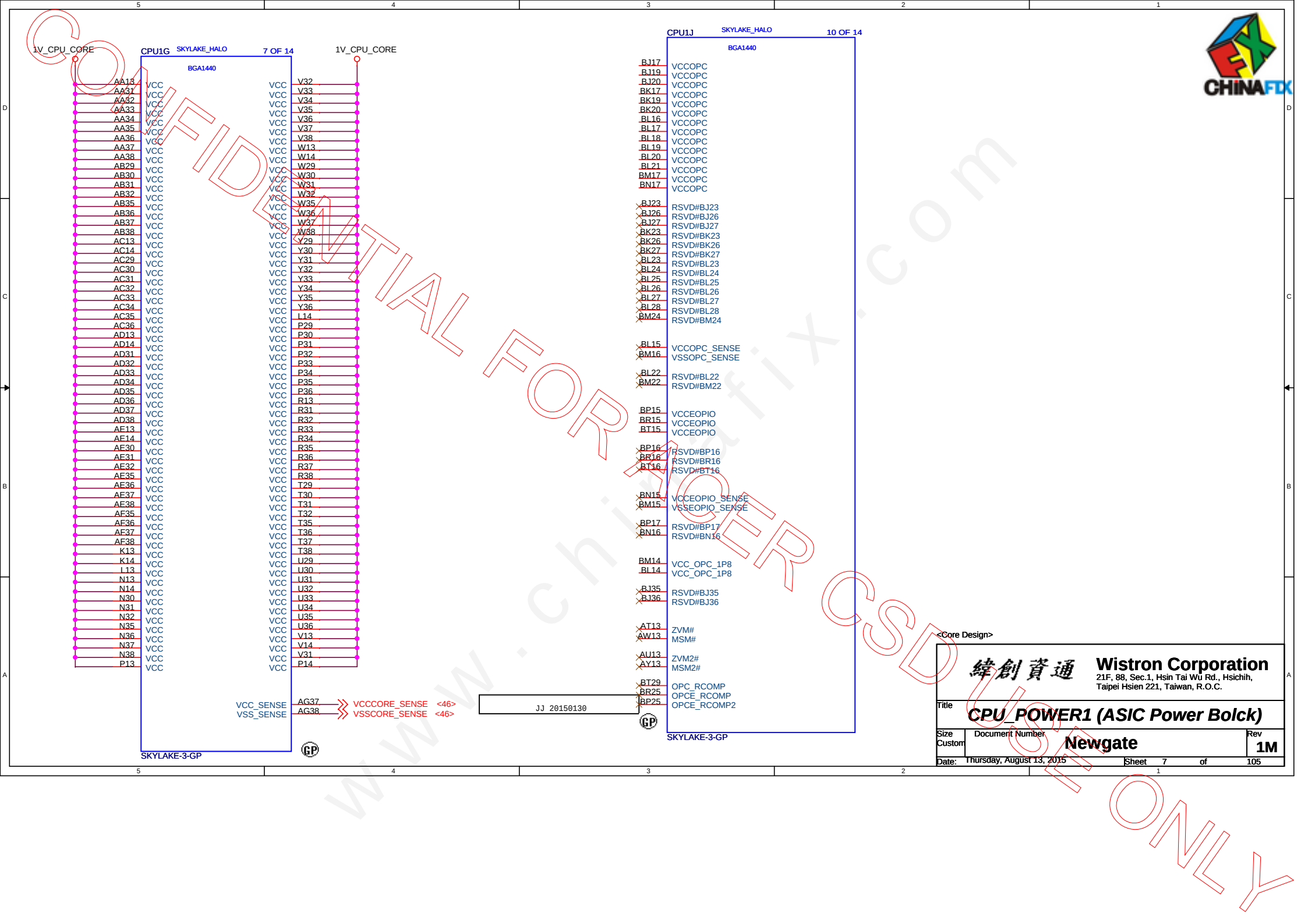
Title: CPU_CFG_CFG STRAP

Size: A2 | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 6 of 109



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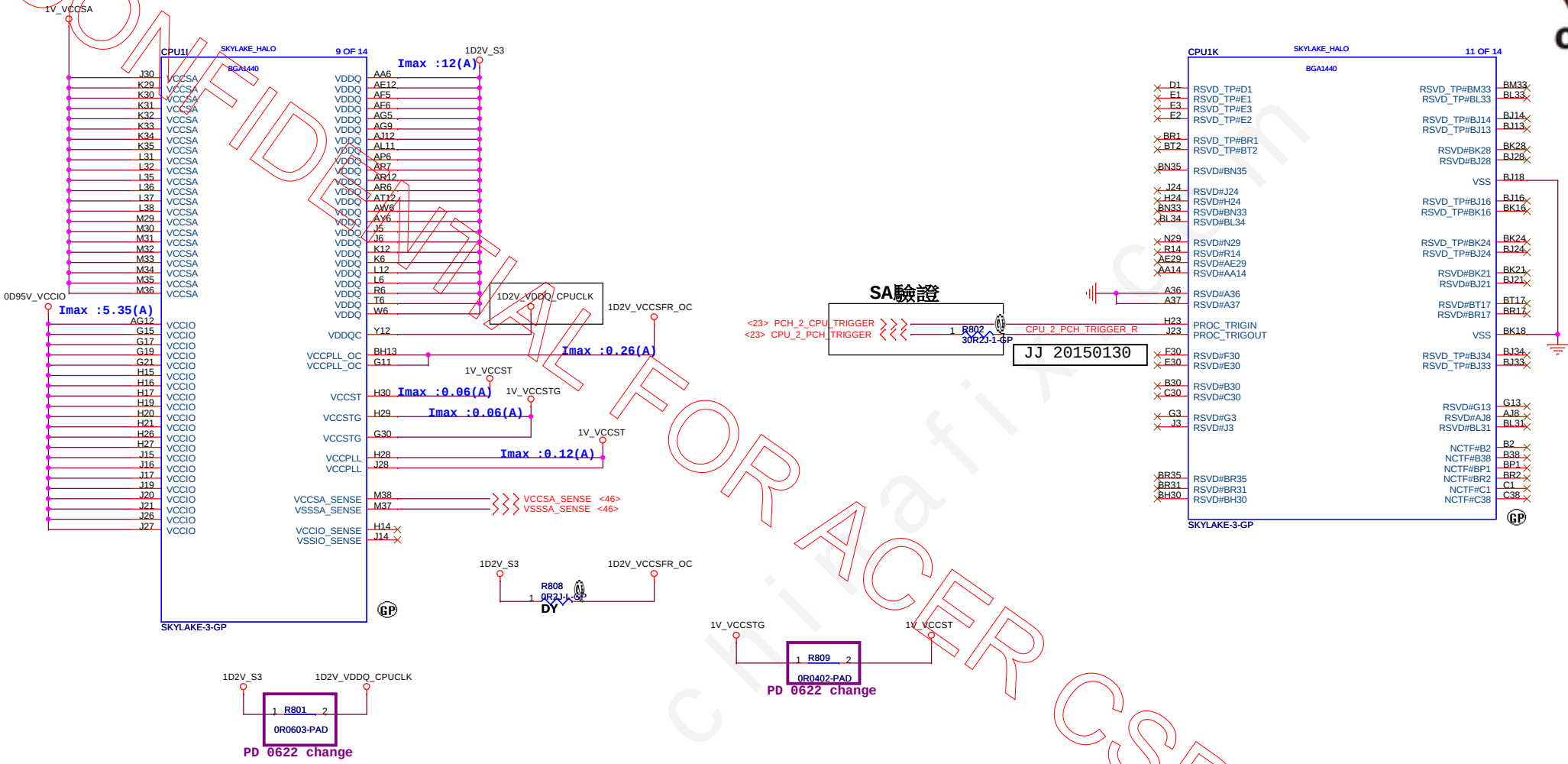
SSID = CPU



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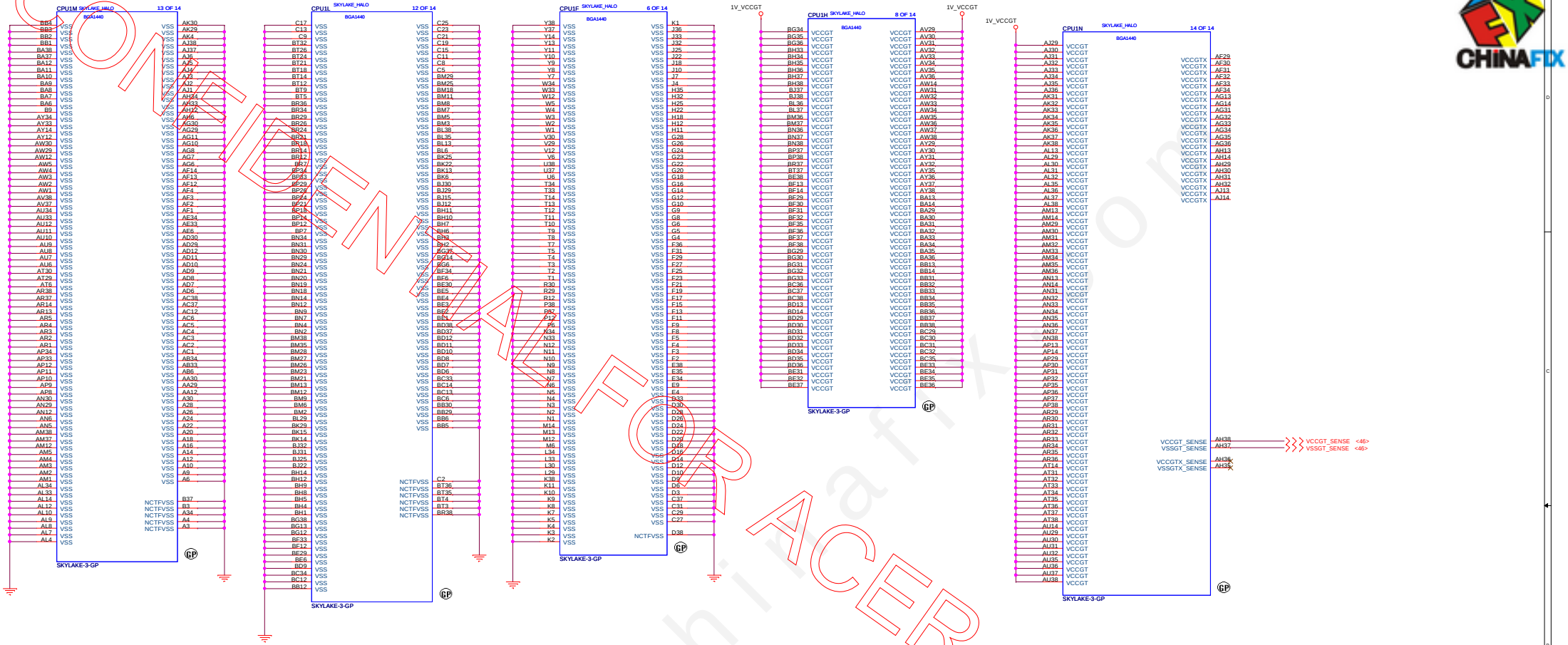
Title: CPU_POWER2(ASIC Power Bolck)

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 8 of 105

SSID = CPU



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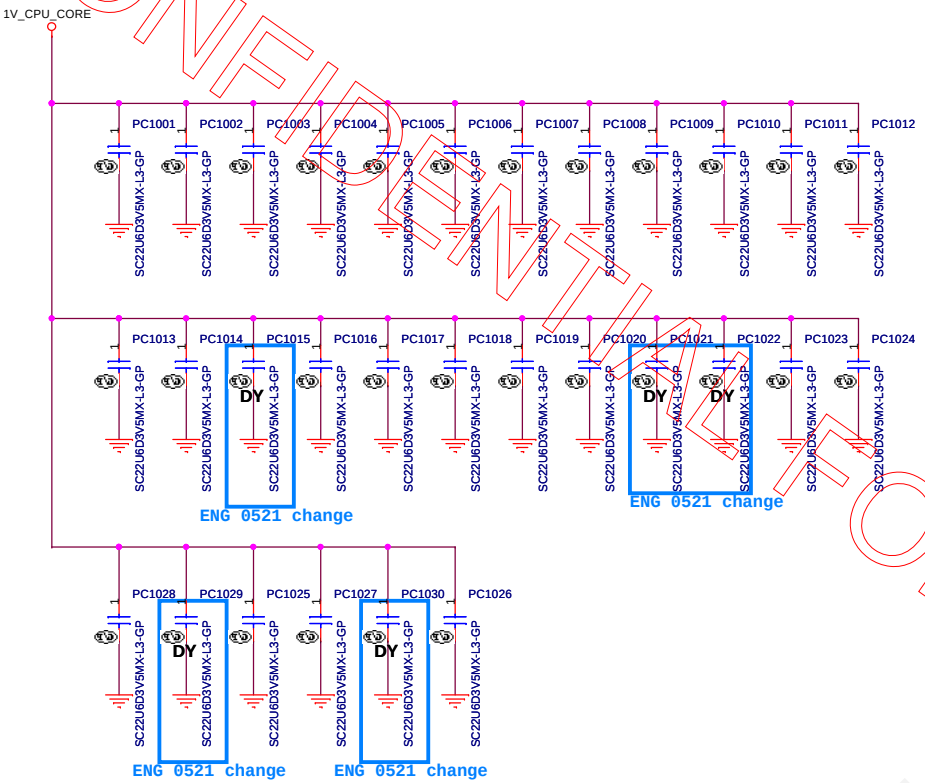
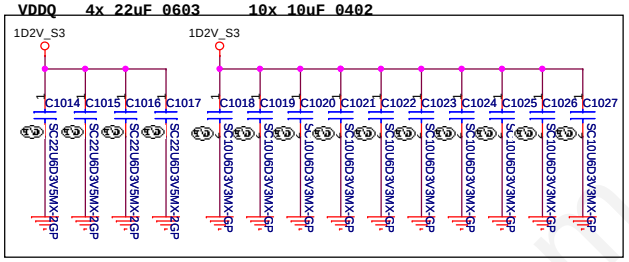
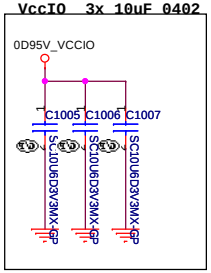
Title: CPU_POWER3(ASIC Power Bolck)

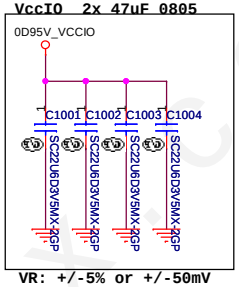
Size: A2 | Document Number: Newgate | Rev: 1M

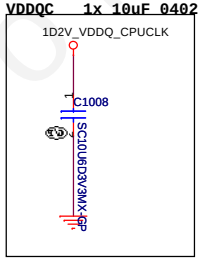
Date: Thursday, August 13, 2015 | Sheet 9 of 105

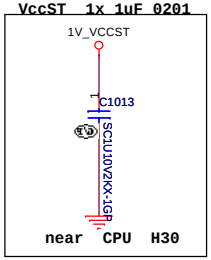




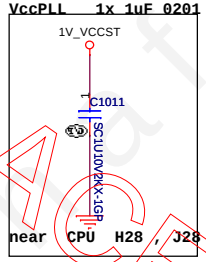


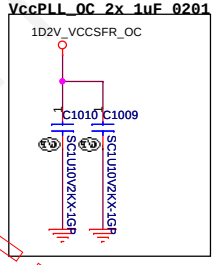


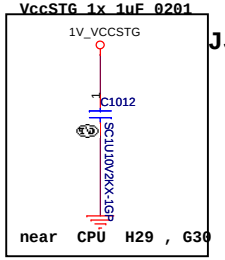




VR: +/-5% or +/-50mV
Place close to VR output







JJ 20150130

Decoupling Requirements for SKL H Processor (Sheet 2 of 2)

Domain	Board Edge cap	Backside cap	Notes
$V_{CC_{GT}}$	6x 47uF 0805		
		8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
$V_{CC_{GTx}}$	8x 22uF 0603		
		4x 10uF 0402	
		12x 1uF 0201	
$V_{CC_{SA}}$	1x 47uF 0805		
		1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
V_{DDQ}		4x 22uF 0603	Share supply with DRAM
		10x 10uF 0402	
V_{DDQC}		1x 10uF 0402	
$V_{CC_{IO}}$	2x 47uF 0805		VR: +/-5% or +/-50mV Place close to VR output
		3x 10uF 0402	
$V_{CC_{ST}}$		1x 1uF 0201	
$V_{CC_{STG}}$		1x 1uF 0201	Share supply with 1.0V PCH rail
$V_{CC_{PLL}}$		1x 1uF 0201	
$V_{CC_{PLL_OC}}$		2x 1uF 0201	Supply from 1.2V V_{DDQ}
$V_{CC_{OPC}}$		10x 10uF 0402	VR: +/-5% or +/-50mV
$V_{CC_{EOPIO}}$		3x 10uF 0402	VR: +/-5% or +/-50mV

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Title: 010_CPU (Power CAP1)

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1V_VCCGT

1V_VCCSA

PC1101 PC1102 PC1103 PC1104 PC1105 PC1106 PC1107 PC1108 PC1109 PC1110

PC1111 PC1112 PC1113 PC1114 PC1115 PC1116 PC1117 PC1118 PC1119 PC1120

PC1121 PC1122 PC1123 PC1124 PC1125 PC1126

PC1127 PC1128 PC1129 PC1130 PC1131 PC1132

PC1148 PC1149 PC1150 PC1151 PC1152

PC1157 PC1153 PC1154 PC1155 PC1156

SC22U6D3V5MX-L3-GP

DY

ENG 0521 change

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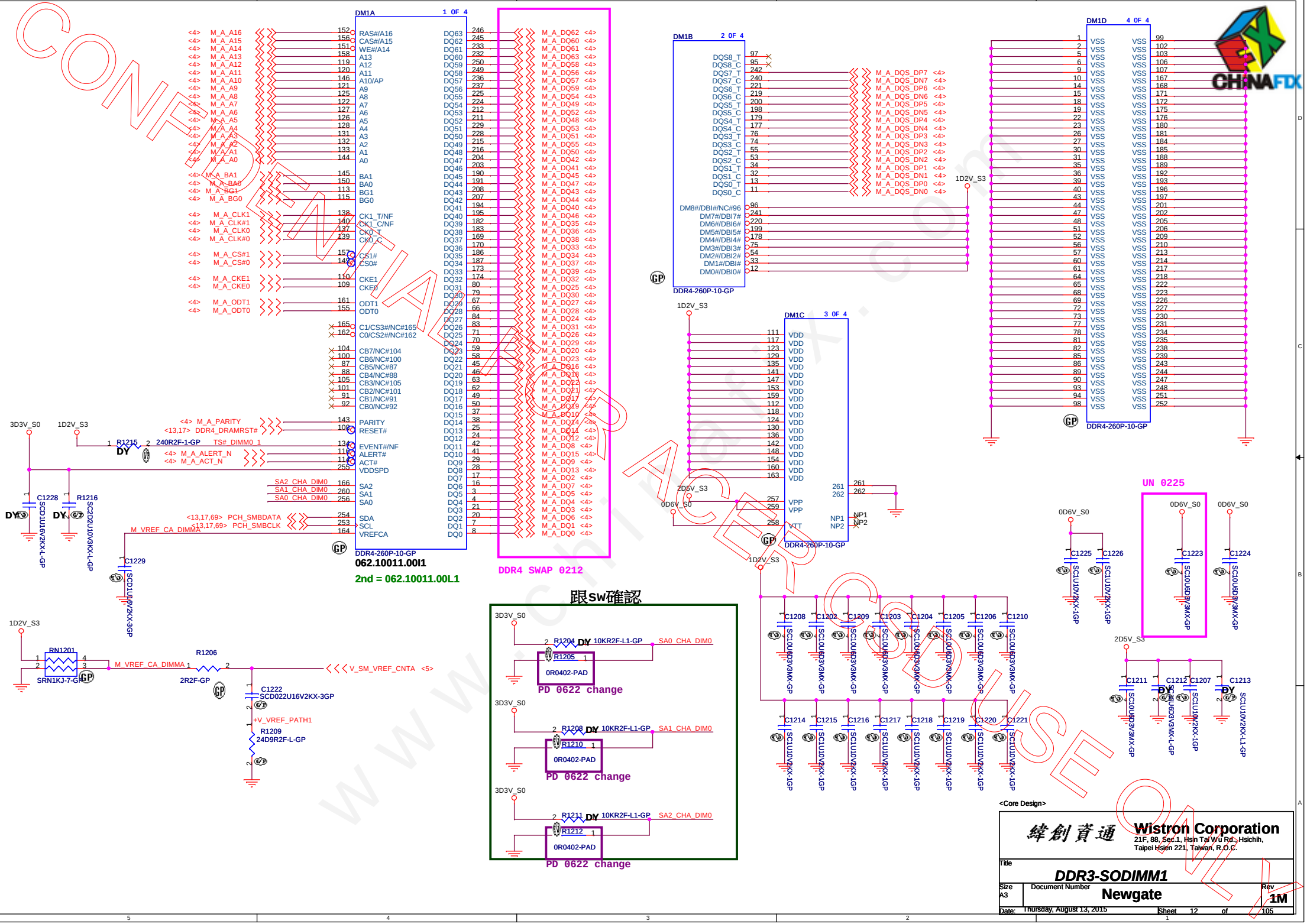
Title: **CPU (Power CAP2)**

Size	Document Number	Rev
A4	Newgate	1M

Date: Wednesday, August 12, 2015 Sheet 11 of 105


DM1A
1 OF 4
DDR4-260P-10-GP
062.10011.00I1
2nd = 062.10011.00L1
DDR4 SWAP 0212
DM1B
2 OF 4
DDR4-260P-10-GP
DM1C
3 OF 4
DDR4-260P-10-GP
DM1D
4 OF 4
DDR4-260P-10-GP
跟Sw確認
PD 0622 change
PD 0622 change
PD 0622 change
UN 0225
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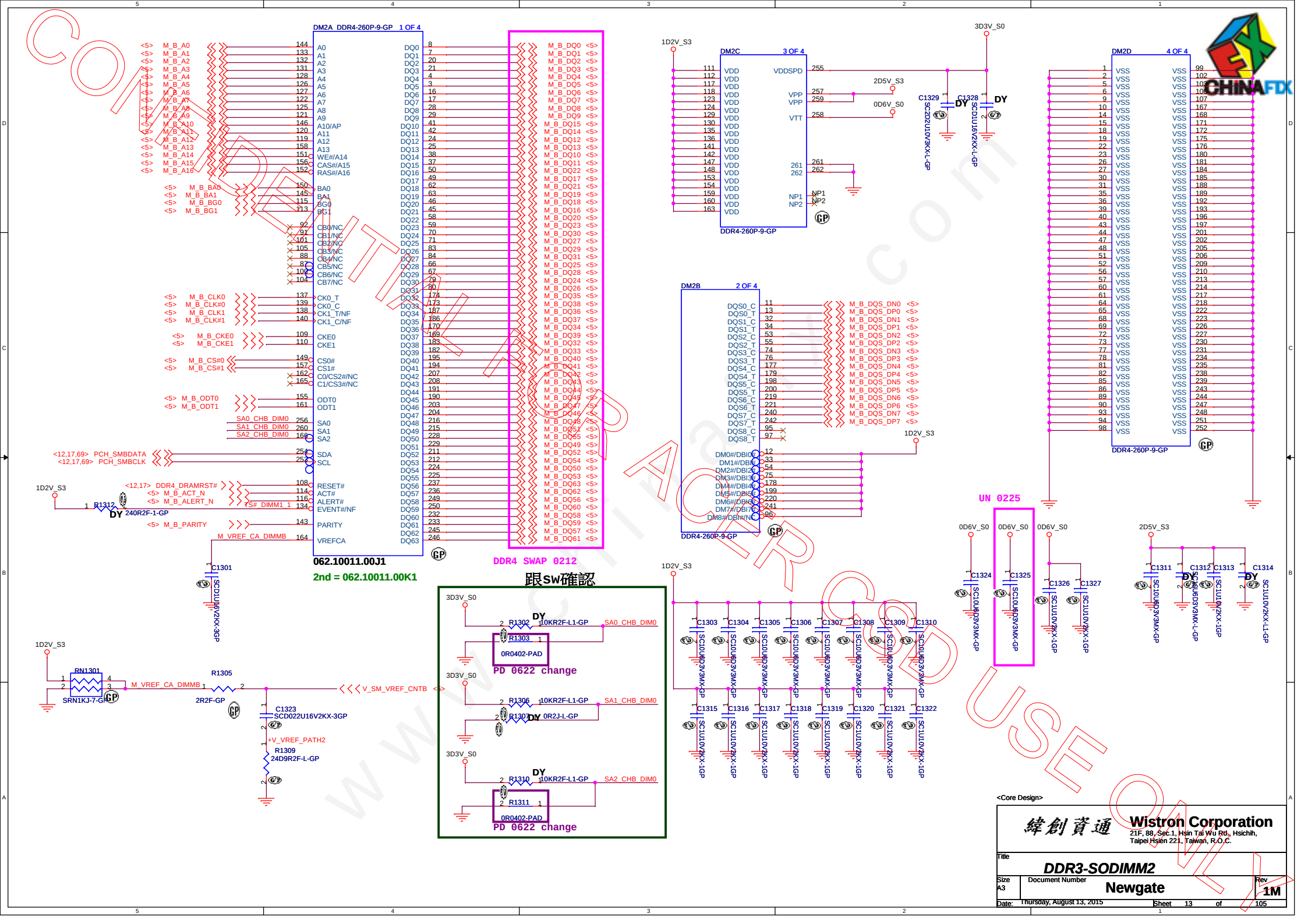
Title
DDR3-SODIMM1
Size A3
Document Number
Newgate
Rev 1M
Date: Thursday, August 13, 2015
Sheet 12 of 105


DM2A DDR4-260P-9-GP 1 OF 4
DM2C 3 OF 4
DM2B 2 OF 4
DM2D 4 OF 4
DDR4-260P-9-GP
062.10011.00J1
2nd = 062.10011.00K1
DDR4 SWAP 0212
跟SW確認
PD 0622 change
PD 0622 change
UN 0225
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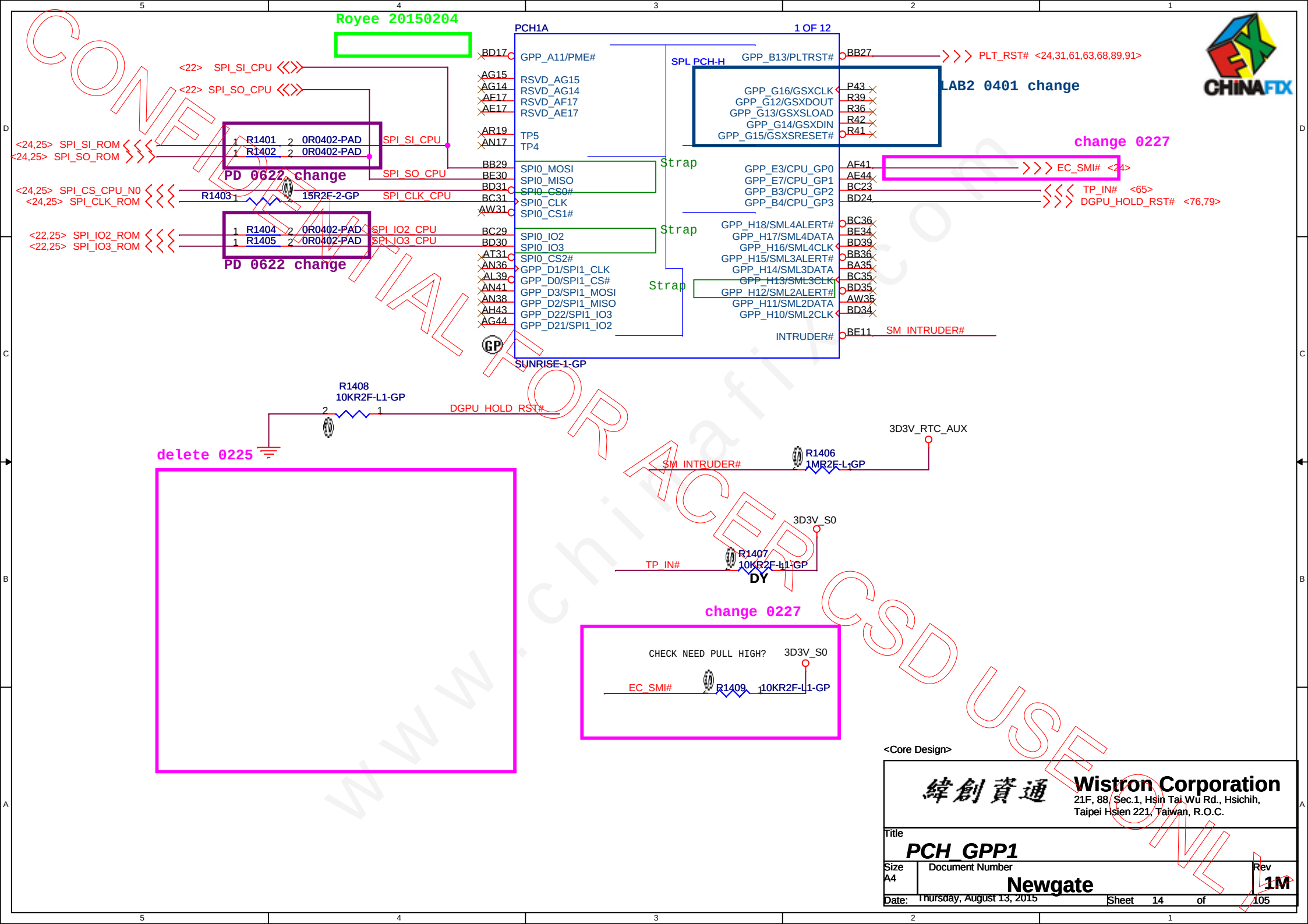
Title
DDR3-SODIMM2
Size A3
Document Number
Newgate
Rev 1M
Date: Thursday, August 13, 2015
Sheet 13 of 105



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Title: PCH_GPP1

Size: A4 | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 14 of 105

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SSID = PCH

PCH1B

2 OF 12

SPL PCH-H

DMI

USB 2.0

PCIe/USB 3

SUNRISE-1-GP

LAB2 0401 change

Delete WIGIG 0204

WIGIG

WIFI

LAN

R1504 100R2F-L3-GP

R1510 10KR2F-L1-GP

R1509 113R2F-GP

3D3V_S5

USB3.0 Port 1 USB Charger

USB3.0 Port 2(USB2.0)

USB3.1 (type C)

USB2.0 (DB)

Bluetooth

LAB2 0401 change

CCD

Card reader

JJ 2015/01/27

RN1501 SRN1KJ-7-GP

USB Table

Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	
4	
5	USB2.0
6	
7	Bluetooth
8	Touch Screen
9	CCD
10	Card reader
11	Finger Printer
12	
13	
14	

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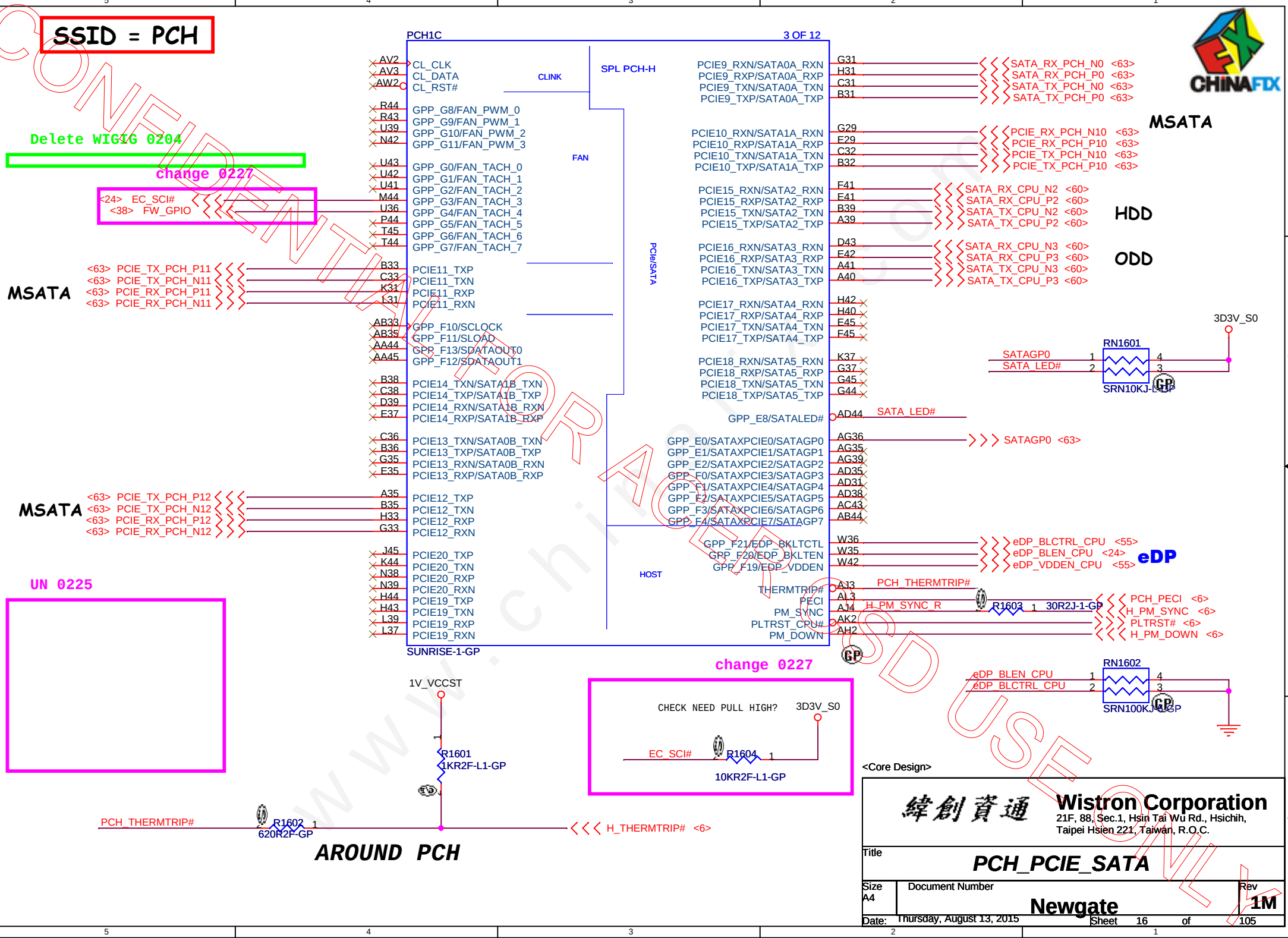
Title: PCH PCIE DMI USB

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 15 of 105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Delete WIGIG 0204
change 0227
<24> EC_SCI#
<38> FW_GPIO
MSATA
<63> PCIE_TX_PCH_P11
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<63> PCIE_RX_PCH_P11
<63> PCIE_RX_PCH_N11
MSATA
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<63> PCIE_RX_PCH_P12
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UN 0225
PCH1C
3 OF 12
SPL PCH-H
CLINK
FAN
PCIe/SATA
HOST
SUNRISE-1-GP
AV2 CL_CLK
AV3 CL_DATA
AW2 CL_RST#
R44 GPP_G8/FAN_PWM_0
R43 GPP_G9/FAN_PWM_1
U39 GPP_G10/FAN_PWM_2
N42 GPP_G11/FAN_PWM_3
U43 GPP_G0/FAN_TACH_0
U42 GPP_G1/FAN_TACH_1
U41 GPP_G2/FAN_TACH_2
M44 GPP_G3/FAN_TACH_3
U36 GPP_G4/FAN_TACH_4
P44 GPP_G5/FAN_TACH_5
T45 GPP_G6/FAN_TACH_6
T44 GPP_G7/FAN_TACH_7
B33 PCIE11_TXP
C33 PCIE11_TXN
K31 PCIE11_RXP
L31 PCIE11_RXN
AB33 GPP_F10/SCLOCK
AB35 GPP_F11/SLOAD
AA44 GPP_F13/SDATAOUT0
AA45 GPP_F12/SDATAOUT1
B38 PCIE14_TXN/SATA1B_TXN
C38 PCIE14_TXP/SATA1B_TXP
D39 PCIE14_RXN/SATA1B_RXN
E37 PCIE14_RXP/SATA1B_RXP
C36 PCIE13_TXN/SATA0B_TXN
B36 PCIE13_TXP/SATA0B_TXP
G35 PCIE13_RXN/SATA0B_RXN
E35 PCIE13_RXP/SATA0B_RXP
A35 PCIE12_TXP
B35 PCIE12_TXN
H33 PCIE12_RXP
G33 PCIE12_RXN
J45 PCIE20_TXP
K44 PCIE20_TXN
N38 PCIE20_RXP
N39 PCIE20_RXN
H44 PCIE19_TXP
H43 PCIE19_TXN
L39 PCIE19_RXP
L37 PCIE19_RXN
PCIE9_RXN/SATA0A_RXN G31
PCIE9_RXP/SATA0A_RXP H31
PCIE9_TXN/SATA0A_TXN C31
PCIE9_TXP/SATA0A_TXP B31
SATA_RX_PCH_N0 <63>
SATA_RX_PCH_P0 <63>
SATA_TX_PCH_N0 <63>
SATA_TX_PCH_P0 <63>
MSATA
PCIE10_RXN/SATA1A_RXN G29
PCIE10_RXP/SATA1A_RXP E29
PCIE10_TXN/SATA1A_TXN C32
PCIE10_TXP/SATA1A_TXP B32
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PCIE_RX_PCH_P10 <63>
PCIE_TX_PCH_N10 <63>
PCIE_TX_PCH_P10 <63>
PCIE15_RXN/SATA2_RXN F41
PCIE15_RXP/SATA2_RXP E41
PCIE15_TXN/SATA2_TXN B39
PCIE15_TXP/SATA2_TXP A39
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SATA_RX_CPU_P2 <60>
SATA_TX_CPU_N2 <60>
SATA_TX_CPU_P2 <60>
HDD
PCIE16_RXN/SATA3_RXN D43
PCIE16_RXP/SATA3_RXP E42
PCIE16_TXN/SATA3_TXN A41
PCIE16_TXP/SATA3_TXP A40
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SATA_RX_CPU_P3 <60>
SATA_TX_CPU_N3 <60>
SATA_TX_CPU_P3 <60>
ODD
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PCIE17_RXP/SATA4_RXP H40
PCIE17_TXN/SATA4_TXN E45
PCIE17_TXP/SATA4_TXP F45
PCIE18_RXN/SATA5_RXN K37
PCIE18_RXP/SATA5_RXP G37
PCIE18_TXN/SATA5_TXN G45
PCIE18_TXP/SATA5_TXP G44
3D3V_S0
RN1601
SATAGP0
SATA_LED#
SRN10KJ-L-GP
GPP_E8/SATALED# AD44
SATA_LED#
GPP_E0/SATAXPCIE0/SATAGP0 AG36
GPP_E1/SATAXPCIE1/SATAGP1 AG35
GPP_E2/SATAXPCIE2/SATAGP2 AG39
GPP_F0/SATAXPCIE3/SATAGP3 AD35
GPP_F1/SATAXPCIE4/SATAGP4 AD31
GPP_F2/SATAXPCIE5/SATAGP5 AD38
GPP_F3/SATAXPCIE6/SATAGP6 AC43
GPP_F4/SATAXPCIE7/SATAGP7 AB44
SATAGP0 <63>
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GPP_F20/EDP_BKLTEN W35
GPP_F19/EDP_VDDEN W42
eDP_BLCTRL_CPU <55>
eDP_BLEN_CPU <24>
eDP_VDDEN_CPU <55>
eDP
THERMTRIP# AJ3
PECI AL3
PM_SYNC AJ4
PLTRST_CPU# AK2
PM_DOWN AH2
PCH_THERMTRIP#
H_PM_SYNC_R
R1603 30R2J-1-GP
PCH_PECI <6>
H_PM_SYNC <6>
PLTRST# <6>
H_PM_DOWN <6>
RN1602
eDP_BLEN_CPU
eDP_BLCTRL_CPU
SRN100KJ-GP
1V_VCCST
R1601
1KR2F-L1-GP
change 0227
CHECK NEED PULL HIGH?
3D3V_S0
EC_SCI#
R1604
10KR2F-L1-GP
PCH_THERMTRIP#
R1602
620R2F-GP
H_THERMTRIP# <6>
AROUND PCH
<Core Design>
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Title
PCH_PCIE_SATA
Size A4
Document Number
Newgate
Rev 1M
Date: Thursday, August 13, 2015
Sheet 16 of 105
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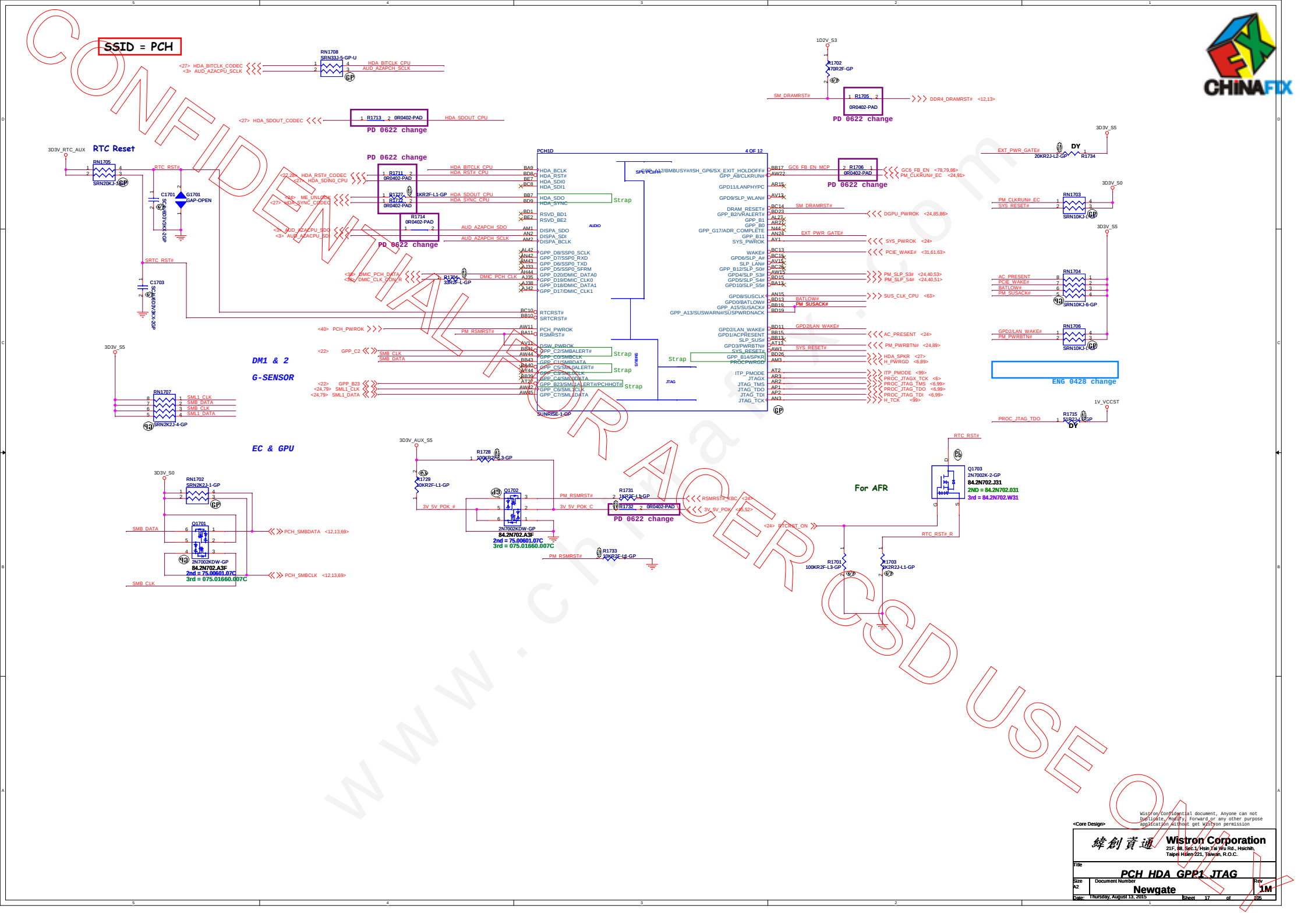

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SSID = PCH

MP 0807 change

MP 0807 change

PCH1F

6 OF 12

SPL PCH-H

SUNRISE-1-GP

LAB2 0401 change

GPIO REVIEW CHECK

GPIO REVIEW CHECK

DEVSLP_PCH <63>

3D3V_S0

RN1806

SRN10KJ-GP

INT_SERIRQ

H_RCIN#

LPC_CLK_CPU_P0

R1809 22R2J-L1-GP

R1810 22R2J-L1-GP

LPC_CLK_KBC <24>

LPC_CLK_DBG <68>

ENG 0417 change

LPC_CLK_CPU_P1

R1805 22R2J-L1-GP

TPM

LPC_CLK_TPM <91>

ENG 0417 change

PEG CLOCK CHECK WITH SW

CHECK P and N

3D3V_S0

R1801 10KR2F-L1-GP PIRQA#

DY

3D3V_S0

RN1802

WLAN_CLKREQ_CPU#

LAN_CLKREQ_CPU#

MSATA_CLKREQ_CPU#

SRN10KJ-GP

RN1805

PEG_CLKREQ_CPU#

TBT_CLKREQ_CPU#

SRN10KJ-GP

1D0V_S5

R1806 2K7R2F-GP

CHECK WITH SW(VGA)

LAB2 0401 change

PCH1G

7 OF 12

SPL PCH-H

SUNRISE-1-GP

LAB2 0401 change

C1803 SC15P50V2JN-2-GP

C1804 SC15P50V2JN-2-GP

X1802

XTAL-24MHZ-135-GP

082.30006.0041

R1808 1MR2F-L-GP

CPU_XTAL_24M_IN

CPU_XTAL_24M_OUT

ENG 0417 change

R1807 10MR2J-L-GP

X1801

XTL-32D768KHZ-6-GP

82.30001.B21

C1801 SC4D7P50V2BN-GP

C1802 SC4D7P50V2BN-GP

XTL_32K_X1_CPU

XTL_32K_X2_CPU

LAB2 0410 change

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Title: PCH_USB3_CLOCK

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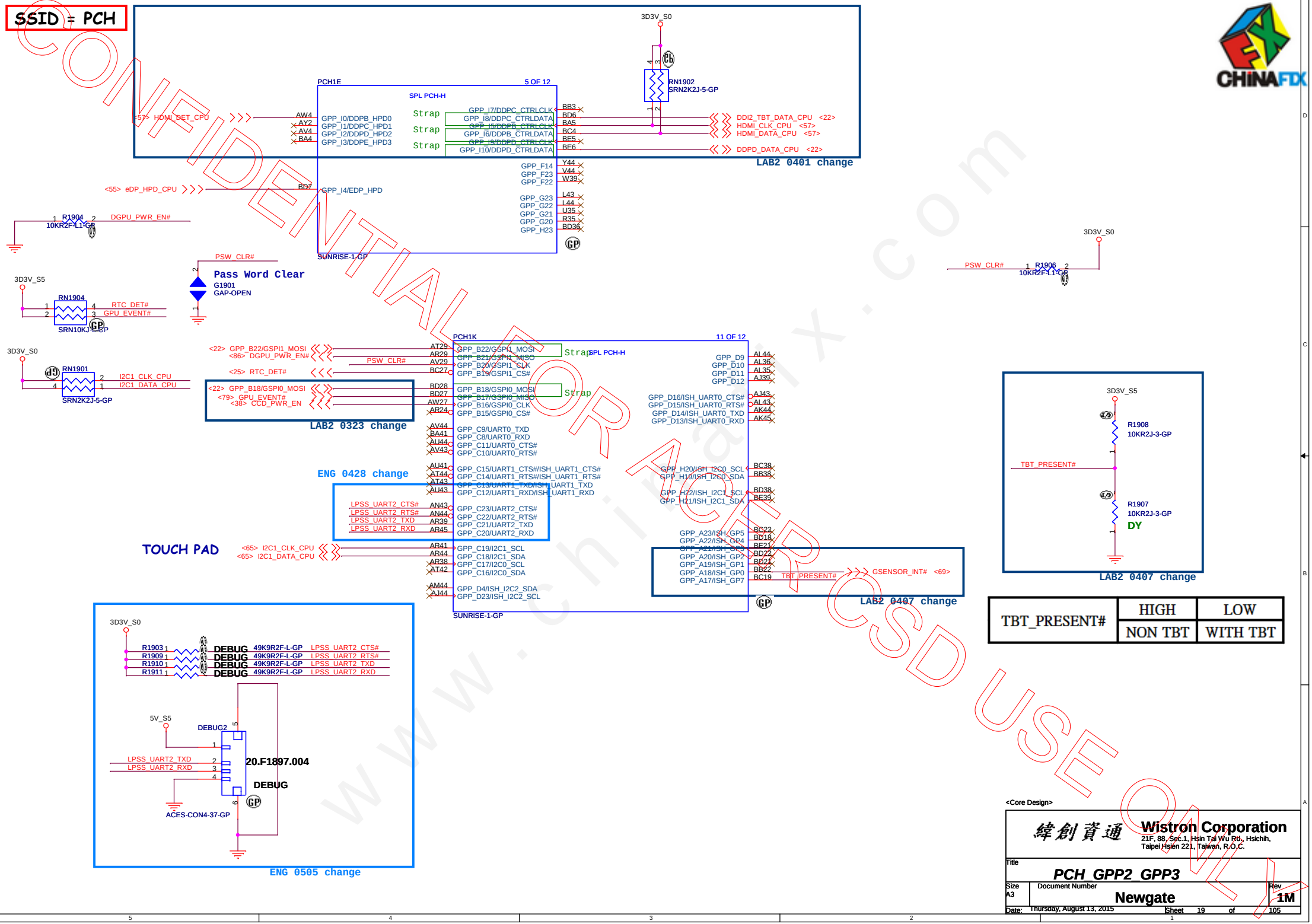

TBT_PRESENT#	HIGH	LOW
	NON TBT	WITH TBT

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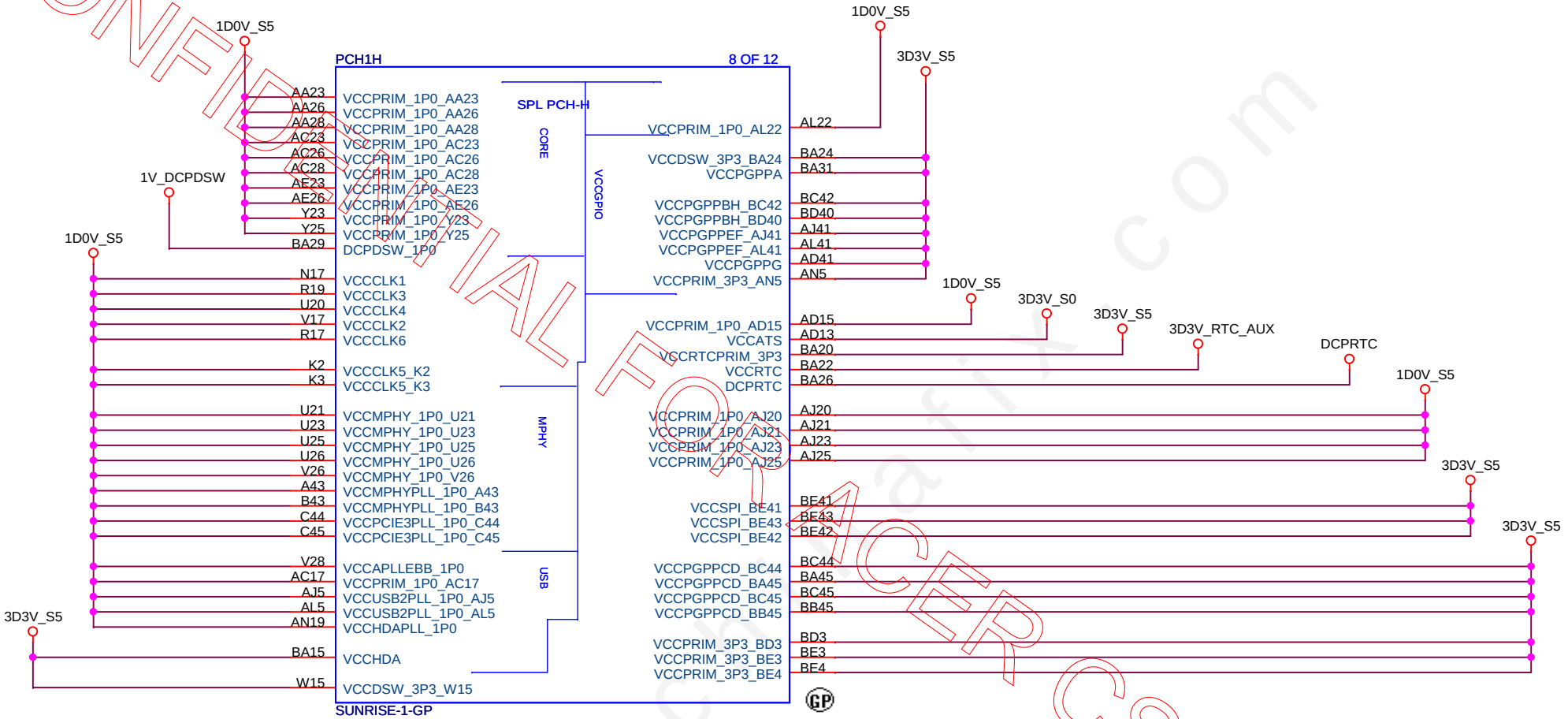
Title: PCH_GPP2_GPP3
Size: A3
Document Number: Newgate
Rev: 1M
Date: Thursday, August 13, 2015
Sheet 19 of 105

SSID = PCH



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Title	***PCH_POWER_VCCPRIM_VCCMPHY***
Size: A4	Document Number: **Newgate**
Rev: **1M**	
Date: Wednesday, August 12, 2015	Sheet 20 of 105

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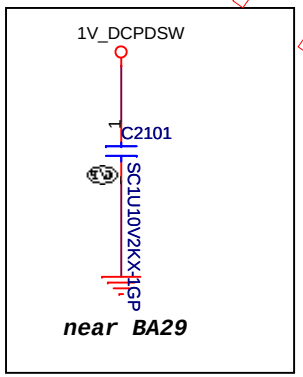
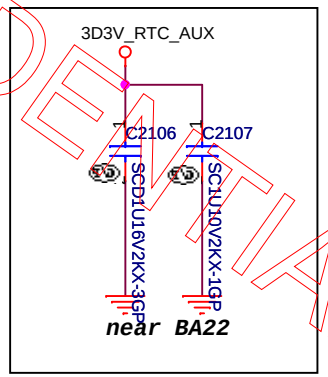
DcpDSW
1x 1uF



VccRTC
1x1 uF 1x0.1 uF



VccRTCPRIM
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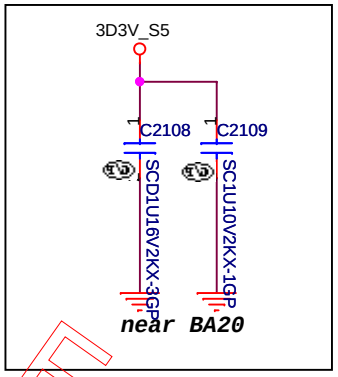
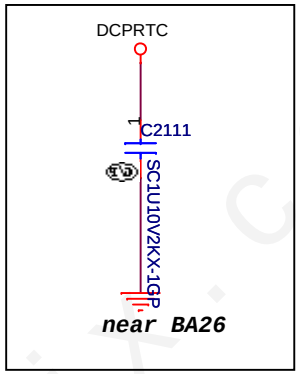
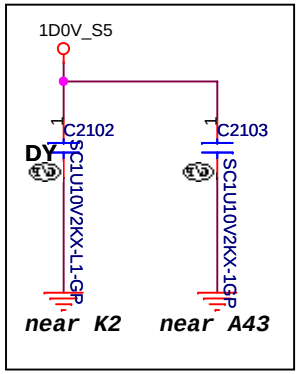


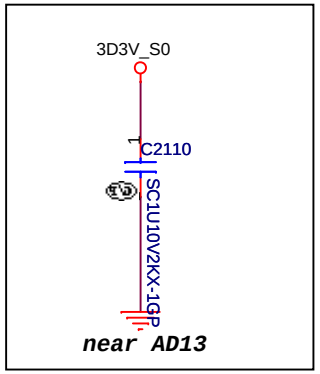
DcpRTC
1x 0.1uF



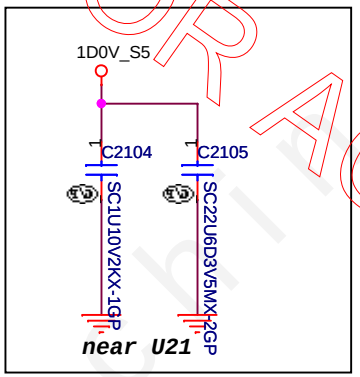
VccMPHYPLL / VccPCIE3PLL
1x1 uF



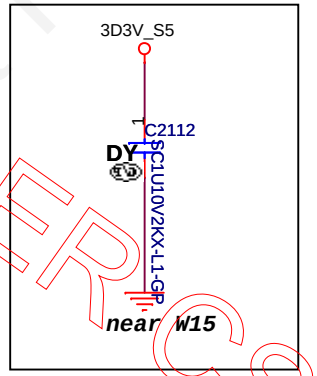
VccATS
1x1 uF



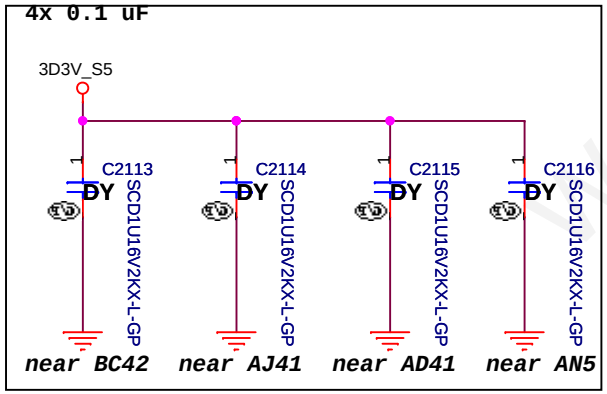
VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG / VccPRIM
4x 0.1 uF



Decoupling and Power Connection Requirements for SKL S/H PCH (DT / AIO) (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)umney / (E)dge	Place capacitor(s) near ball(s)
V1.0A	VccMPHY VccPRIM VccAPLLEBB	U21, U23, U25, U26, V26, AC17, V28	1 uF	0402	1	E (<3 mm)	U21
			22 uF	0805	1	E (<5 mm)	
	VccMPHYPLL VccPCIE3PLL	A43, B43, C44, C45	1 uF	0402	1	E (<5 mm)	A43
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL VccHDAPLL	AJ5, AL5, AN19	-	-	-	-	-
	VccPRIM	AL22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA26, AA28, AC23, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
V1.0DSW	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)	BA29
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AL41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccPGPPA	BA31	-	-	-	-	-
	VccSPI	BE41, BE42, BE43	-	-	-	-	-
	VccPGPPD	BC44, BA45, BC45, BB45	-	-	-	-	-
V1.8A/ V1.85/ V3.3S	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
V1.5A/ V1.8A/ V3.3A	VccHDA	BA15	-	-	-	-	-
V3.3A	VccRTCPRIM	BA20	1 uF	0402	1	E (<5 mm)	BA20
			0.1 uF	0402	1	E (<3 mm)	
	VccPRIM	BD3, BE3, BE4	-	-	-	-	-
V3.3RTC	VccRTC	BA22	1 uF	0402	1	E (<5 mm)	BA22
			0.1 uF	0402	1	E (<3 mm)	
V3.3DSW	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

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Title: **PCH_POWER_CAP1**

Size: A4 | Document Number: **Newgate** | Rev: **1M**

Date: Wednesday, August 12, 2015 | Sheet 21 of 105

SSID = PCH

Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic	Pull up at p.71 RN7101	3D3V_S0 R2208 2K2R2J-L1-GP DY LAB2 0401 change DDI2_TBT_DATA_CPU <19>	3D3V_S0 R2201 2K2R2J-L1-GP DY DDPD_DATA_CPU <19>	3D3V_S0 R2202 4K7R2J-L-GP DY GPP_B18/GSPI0_MOSI <19>	3D3V_S5 R2203 4K7R2J-L-GP DY GPP_B22/GSPI1_MOSI <19>		
High	Detected	Detected	Detected	Enable	LPC	Disable	1:SLAVE ATTACEHD FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

Description	Top Swap Override	eSPI or LPC	TLS Confi-dentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23
Schematic			3D3V_S5 R2204 4K7R2J-L-GP DY GPP_C2 <17>	3D3V_S5 RN2201 SRN1KJ-7-GP SPI_IO3_ROM <14,25> SPI_IO2_ROM <14,25> PD 0703 change		3D3V_S5 R2205 20KR2F-L-GP DY SPI_SI_CPU <14>	3D3V_S5 R2206 20KR2F-L-GP DY SPI_SO_CPU <14>	3D3V_S5 R2207 4K7R2J-L-GP DY GPP_B23 <17>
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

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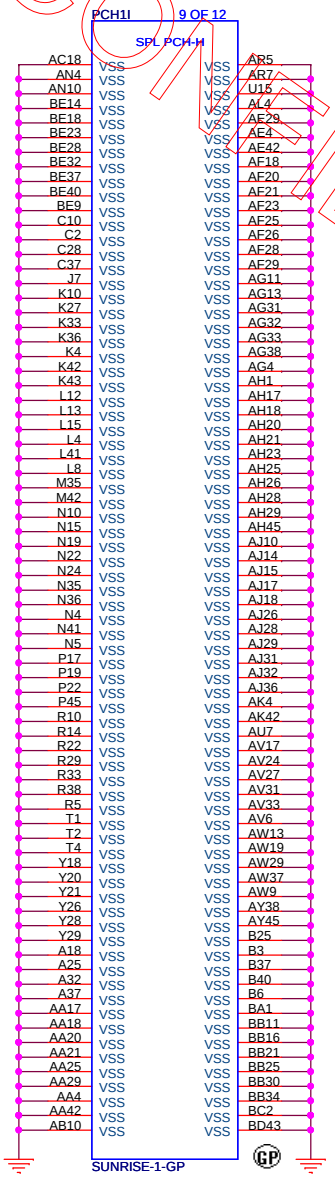
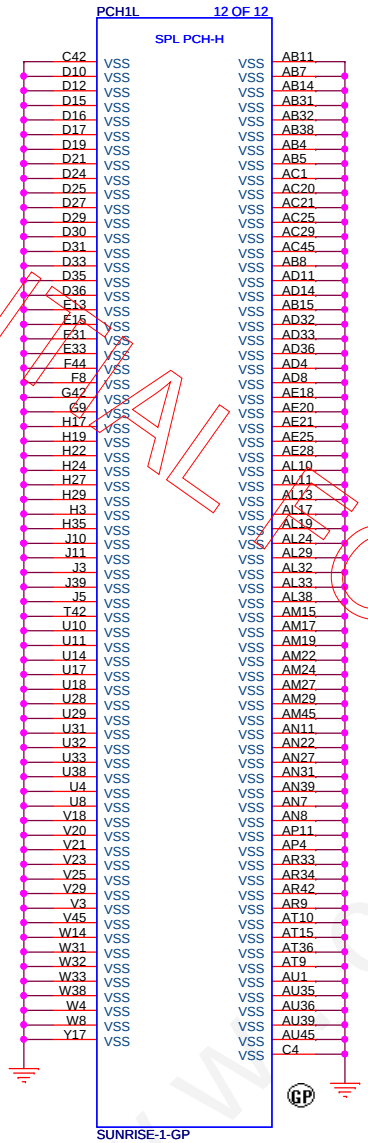
Title: PCH_STRAP

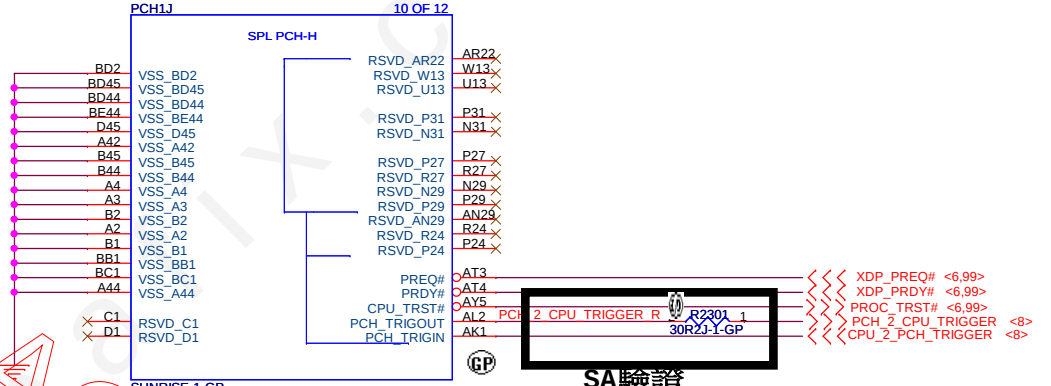
Size: A2 | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 22 of 105

SSID = PCH







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Title: PCH_RSVD_VSS

Size: B | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 23 of 105

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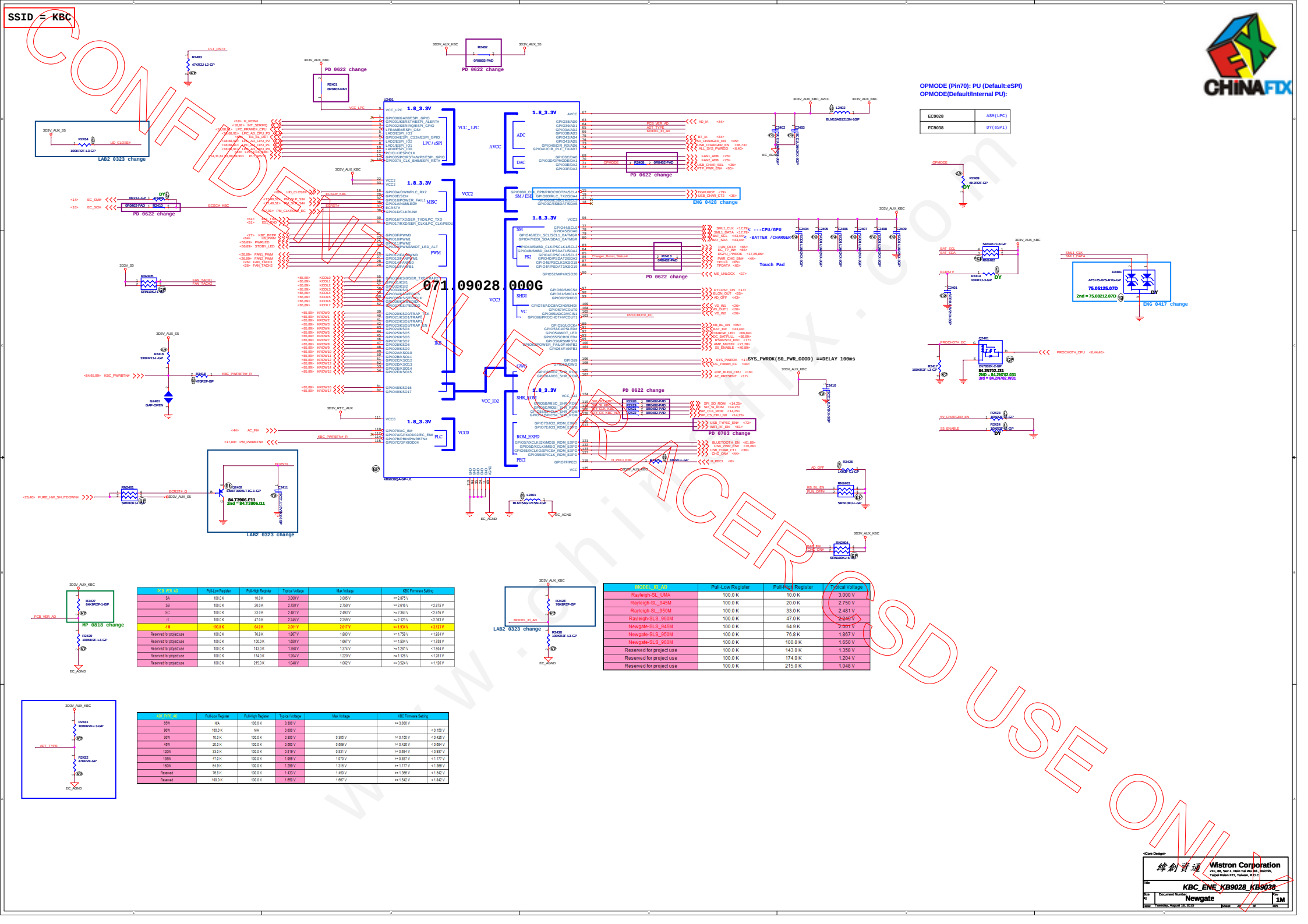
SSID = KBC



PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.393 V	< 2.616 V
-Y	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.393 V
1M	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.880 V	>= 1.739 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.739 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Rayleigh-SL_UMA	100.0 K	10.0 K	3.000 V
Rayleigh-SL_945M	100.0 K	20.0 K	2.750 V
Rayleigh-SL_950M	100.0 K	33.0 K	2.481 V
Rayleigh-SLS_960M	100.0 K	47.0 K	2.245 V
Newgate-SLS_945M	100.0 K	64.9 K	2.001 V
Newgate-SLS_950M	100.0 K	76.8 K	1.867 V
Newgate-SLS_960M	100.0 K	100.0 K	1.650 V
Reserved for project use	100.0 K	143.0 K	1.358 V
Reserved for project use	100.0 K	174.0 K	1.204 V
Reserved for project use	100.0 K	215.0 K	1.048 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	N/A	100.0 K	0.000 V		>= 0.000 V	
90W	100.0 K	N/A	0.000 V			< 0.150 V
30W	10.0 K	100.0 K	0.300 V	0.305 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.684 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.684 V	< 0.937 V
135W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
150W	64.9 K	100.0 K	1.298 V	1.316 V	>= 1.177 V	< 1.386 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.386 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.842 V

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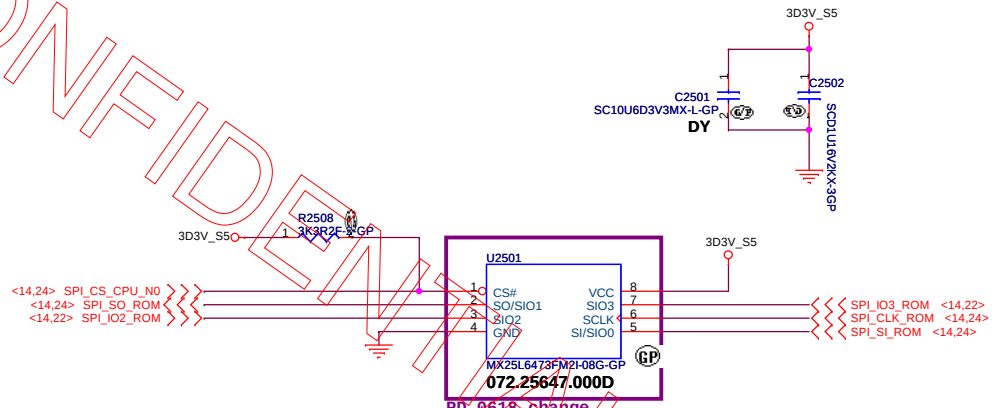
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



SPI FLASH ROM (8M byte) for PCH

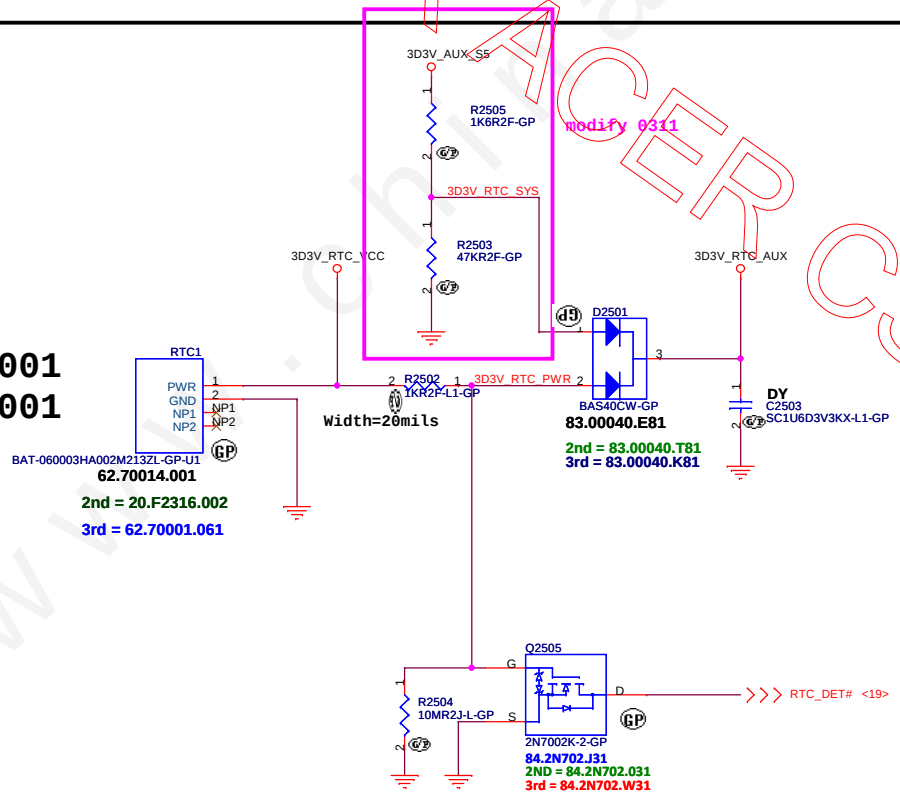
SPI ROM Equal length need to less than 500mil

SPI FLASH ROM (8M byte)

1st = 072.25647.000D (MXIC MX25L6473FM2I-08G)
2nd= 072.25Q64.0F01 (MICRON N25Q064A13ESED0F)
3rd= 72.25Q64.K01 (WINBOND W25Q64FVSSIQ)

Main Func = RTC

RTC BATTERY
1st= 23.22065.001
2nd= 23.20068.001



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Title: Flash(KBC+PCH)/RTC

Size: A3 | Document Number: Newgate | Rev: 1M

Date: Thursday, August 13, 2015 | Sheet 25 of 105

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SSID = Thermal

Layout 15 mil

Layout 15 mil

ADB (Active Dusting Blower) function

AFTP TESTPOINT

FAN_TACH1_C
FAN_TACH2_C

FAN1 conn change by Royee 20150202

FAN2 conn change by Royee 20150202

FOR CPU T8

FOR SYSTEM

PD 0622 change

PD 0622 change

PD 0622 change

PD 0622 change

T8 = 85 degree

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Title: Thermal T8 and FAN
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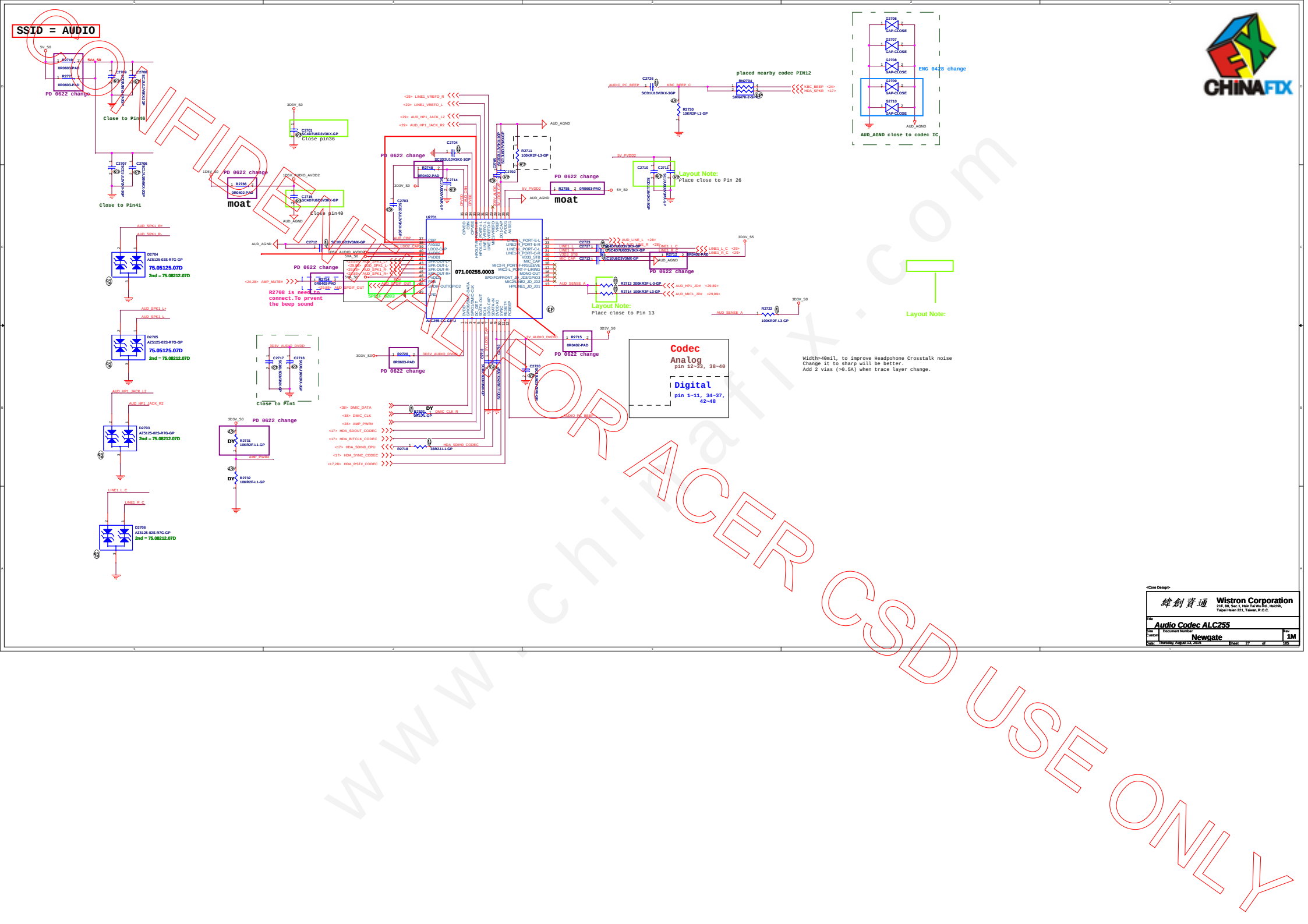
SSID = AUDIO
placed nearby codec PIN12
ENG 0428 change
AUD_AGND close to codec IC
PD 0622 change
Close to Pin46
Close to Pin41
Close pin36
Close pin40
Close to Pin1
moat
Layout Note:
Place close to Pin 26
Layout Note:
Place close to Pin 13
Layout Note:
R2708 is need to connect.To prvent the beep sound
071.00255.0003
ALC255-CG-GR-U
Codec
Analog
pin 12~33, 38~40
Digital
pin 1~11, 34~37, 42~48
Width>40mil, to improve Headpohone Crosstalk noise
Change it to sharp will be better.
Add 2 vias (>0.5A) when trace layer change.
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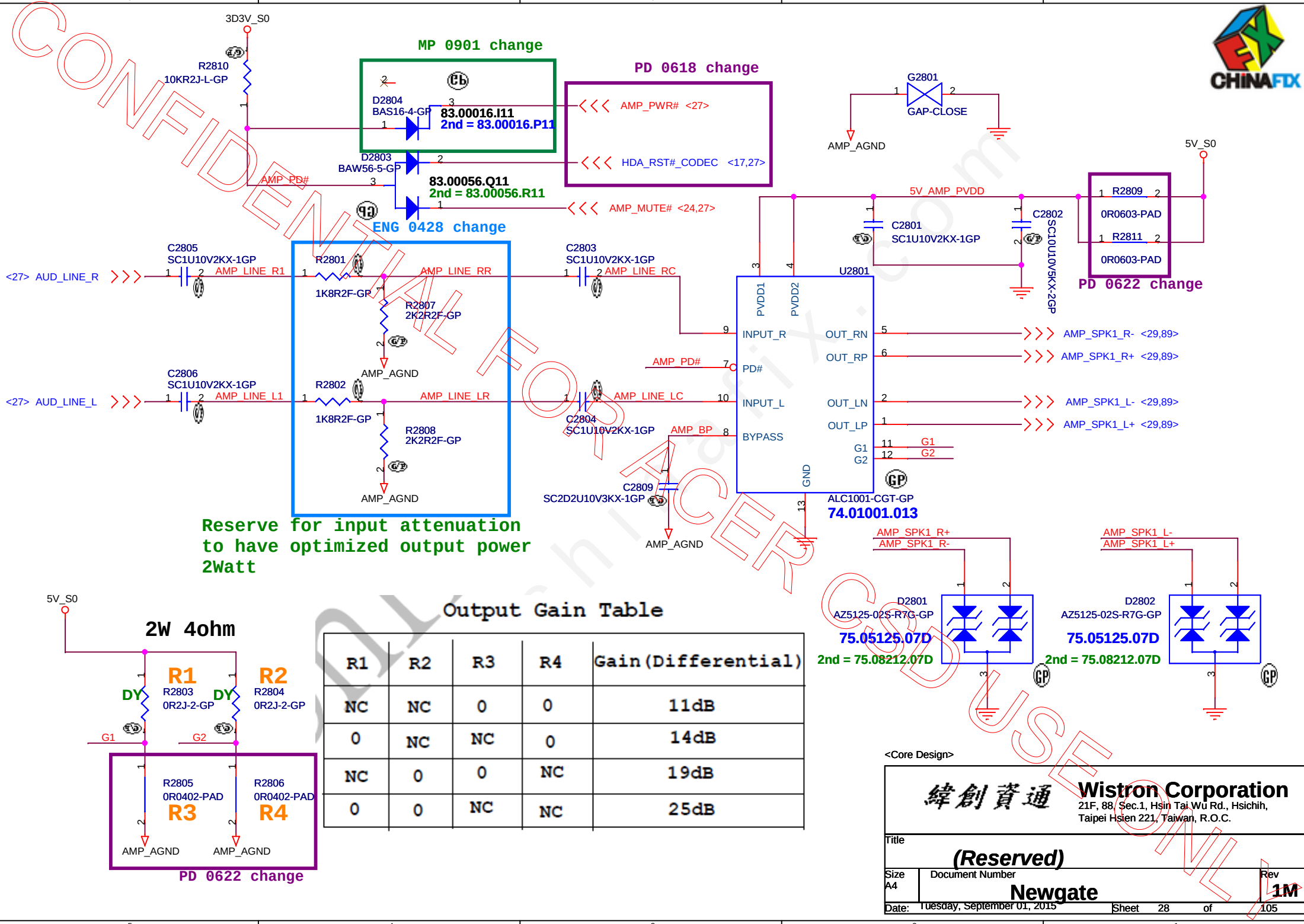
Audio Codec ALC255
Newgate
1M
Thursday, August 11, 2005
27
105



Output Gain Table

R1	R2	R3	R4	Gain(Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

<Core Design>

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Title: (Reserved)

Size: A4 | Document Number: Newgate | Rev: 1M

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SSID = AUDIO

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Speaker

<27,89> AMP_SPK1_L-
<28,89> AMP_SPK1_L+
<27,89> AUD_SPK1_L-
<27,89> AUD_SPK1_L+
<28,89> AMP_SPK1_R-
<28,89> AMP_SPK1_R+
<27,89> AUD_SPK1_R-
<27,89> AUD_SPK1_R+

SPK1
ACES-CON8-12-GP-U1
20.F0818.008

12/17

Layout Note:
Trace width=40mil

EC2906 EC2905 EC2904 EC2903 EC2916 EC2917 EC2918 EC2919
DY
SC1KP50V2KX-1-GP

1nd = 20.F0818.008
2nd = 20.F2348.008

AMP_SPK1_L- <28,89>
AMP_SPK1_L+ <28,89>
AUD_SPK1_L- <27,89>
AUD_SPK1_L+ <27,89>
AMP_SPK1_R- <28,89>
AMP_SPK1_R+ <28,89>
AUD_SPK1_R- <27,89>
AUD_SPK1_R+ <27,89>

AFTP TESTPOINT

AUD_HP1_JACK_R2_OUT <89>
AUD_HP1_JACK_L2_OUT <89>
LINE1_L_IN <89>
LINE1_R_IN <89>
AUD_HP1_JD# <27,89>
AUD_MIC1_JD# <27,89>
5V_SPDIF_S0 <89>
AUD_SPDIF_OUT <27,89>

AFTP TESTPOINT

LINE OUT

PD 0622 change

<27> AUD_HP1_JACK_R2
<27> AUD_HP1_JACK_L2
R2904 R2905 0R3D4R3F-GP
ENG 0504 change
AUD_HP1_JACK_R2_R
AUD_HP1_JACK_L2_R
R2908 R2909 0R0402-PAD
AUD_HP1_JACK_R2_OUT
AUD_HP1_JACK_L2_OUT
<27,89> AUD_HP1_JD#
5V_SPDIF_S0
<27,89> AUD_SPDIF_OUT
C2922 C2923 DY SC100P50V2JN-3GP
AUD_AGND

SPDIF1
M6 M1 M4 M5 M7
LED
A B C
DRIVE IC
TX
AUDIO-JK530-GP-U
022.10033.0011
ENG 0504 change

SCHEMATIC
M6 M1 M4 M5 M7
LED DRIVE IC Tx
A GND B VCC C Vin

MIC IN

PD 0622 change

<27> LINE1_VREFO_L
<27> LINE1_VREFO_R
<27> LINE1_L_C
<27> LINE1_R_C
R2906 R2907 R2901 R2902 2K2R2J-L1-GP 2KR2F-L1-GP
LINE1_L_R
LINE1_R_R
R2910 R2911 0R0402-PAD
LINE1_L_IN
LINE1_R_IN
<27,89> AUD_MIC1_JD#
C2924 C2925 DY SC100P50V2JN-3GP
AUD_AGND

ENG 0504 change
MICIN1
M5 M4 M3 M1 MP MQ NP1 NP2
AUDIO-JK528-GP-U1
022.10002.00J1

SCHEMATIC
SCHEMATIC (PLUG IN)
M5 M4 M3 M1 MP MQ

U2901

5V_S0
AUD_HP1_JD#
IN EN# OUT GND OC#
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
C2920 SCD1U16V2ZY-2GP DY
C2921 SCD1U16V2ZY-2GP DY
5V_SPDIF_S0
R2903 DY 0R2J-2-GP
LAB2 0407 change

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Title: Speaker/ALC255
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PD 0622 change

R3101 0R0603-PAD

REGOUT — 1V_LAN_VDD10

C3102 SCD1U16V2KX-3GP

C3127 C3130 C3125 C3126 C3124 SCD1U16V2KX-L-GP

C3114 SCD1U16V2KX-L-GP

RSET — R3102 2K49R2F-2-L-GP

U3101 RTL8111H-CG-1-GP

3D3V_LAN_VDD33			
1V_LAN_VDD10	3 AVDD10	MDIP0 1	MDI0+ <32>
	8 AVDD10	MDIN0 2	MDI0- <32>
	30 AVDD10	MDIP1 4	MDI1+ <32>
		MDIN1 5	MDI1- <32>
	11 AVDD33	MDIP2 6	MDI2+ <32>
	32 AVDD33	MDIN2 7	MDI2- <32>
		MDIP3 9	MDI3+ <32>
1V_LAN_VDD10	22 DVDD10	MDIN3 10	MDI3- <32>
3D3V_LAN_VDD33	23 VDDREG	CKXTAL1 28	LAN_XTAL_25M_IN
		CKXTAL2 29	LAN_XTAL_25M_OUT
<15> PCIE_TX_PCH_P4 — C3120 SCD1U16V2KX-3GP — PCIE_TX_CON_P4	13 HSIP	REGOUT 24	REGOUT
<15> PCIE_TX_PCH_N4 — C3119 SCD1U16V2KX-3GP — PCIE_TX_CON_N4	14 HSIN	RSET 31	RSET
<15> PCIE_RX_PCH_P4 — C3108 SCD1U16V2KX-3GP — PCIE_RX_CON_P4	17 HSOP	LED0 27	LAN_LED0 — TP3101
<15> PCIE_RX_PCH_N4 — C3107 SCD1U16V2KX-3GP — PCIE_RX_CON_N4	18 HSON	LED1/GPO 26	LAN_LED1 — TP3102
		LED2 25	LAN_LED2 — TP3103
<18> LAN_CLK_CPU	15 REFCLK_P	ISOLATE# 20	ISOLATEB
<18> LAN_CLK_CPU#	16 REFCLK_N	LANWAKE# 21	PCIE_WAKE# <17,61,63>
<18> LAN_CLKREQ_CPU#	12 CLKREQ#		
<14,24,61,63,68,89,91> PLT_RST#	19 PERST#	GND 33	

TP3101 TP3102 TP3103

3D3V_S5 — R3104 0R0805-PAD — 3D3V_LAN_VDD33

PD 0622 change

C3117 SC47U6D3V3KX-L-GP DY

C3118 SC4D7U6D3V3KX-L-GP DY

C3109 C3110 SCD1U16V2KX-3GP

3D3V_S0 — R3107 1KR2J-L2-GP — ISOLATEB — R3108 15K4R2F-GP

X3101 XTAL-25MHZ-181-GP

LAN_XTAL_25M_IN — R3109 1MR2J-L3-GP DY — LAN_XTAL_25M_OUT

C3122 SC12P50V2JN-3GP

C3123 SC15P50V2JN-L-GP

82.30020.G71

2nd = 82.30020.D41

3rd = 082.30005.0231

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Title: LAN(RTL8111)

Size: A3 | Document Number: Newgate | Rev: 1M

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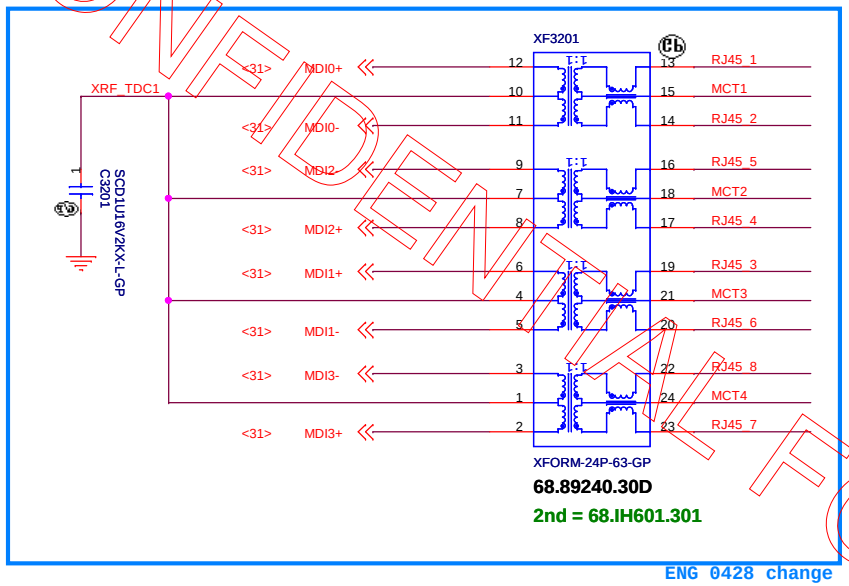
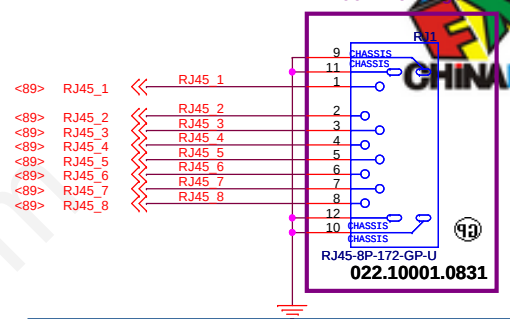
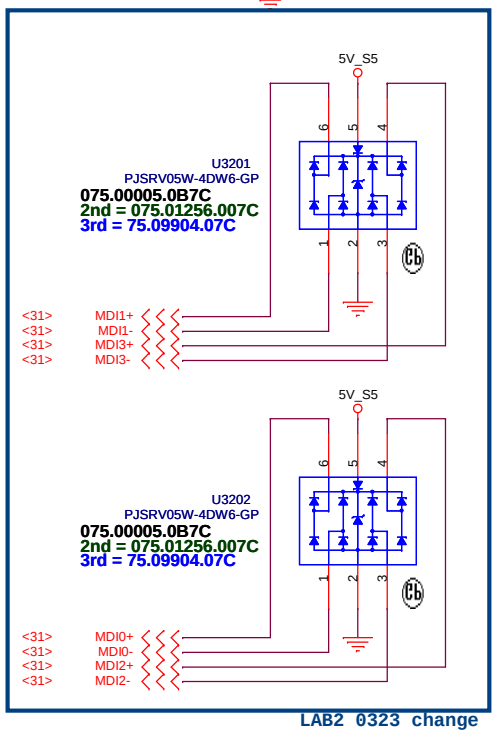
SSID = LAN



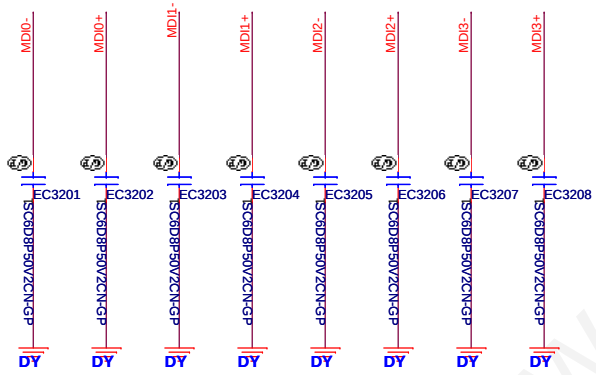
ENG 0428 change

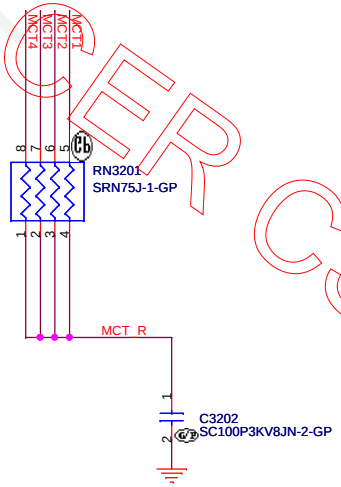
PD 0624 change





LAB2 0323 change





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Title: RJ45+Transformer

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Title
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Title: ***CPU_CFG_CFG STRAP***

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Low Active 2A

5V_S5

C3501 SC1U10V2KX-L1-GP

U3501 SY6288DAAC-GP

IN, EN#, OUT, GND, OC#

074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F

5V_USB30

C3502 SC1U16V2KX-L-GP

C3503 SC100U6D3V6MX-GP

<24,66> USB_PWR_EN#

AFTP TESTPOINT

USB30_RX_CON_N1 <89>
USB30_RX_CON_P1 <89>
USB30_TX_CON_N1 <89>
USB30_TX_CON_P1 <89>
USB_CON_PN1 <89>
USB_CON_PP1 <89>
USB30_RX_CON_N2 <89>
USB30_RX_CON_P2 <89>
USB30_TX_CON_N2 <89>
USB30_TX_CON_P2 <89>
USB_CON_PN2 <89>
USB_CON_PP2 <89>

USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

PD 0701 change

<18> USB30_RX_CPU_N1
<18> USB30_RX_CPU_P1
FR3501 0R0402-PAD → USB30_RX_CON_N1
FR3502 0R0402-PAD → USB30_RX_CON_P1
FC3516 SC1P50V2CN-1GP DY
FC3503 SC1P50V2CN-1GP DY

PD 0701 change

<18> USB30_TX_CPU_N1
<18> USB30_TX_CPU_P1
C3508 SCD1U16V2KX-L-GP
C3509 SCD1U16V2KX-L-GP
USB30_TX_N1_R
USB30_TX_P1_R
FR3504 0R0402-PAD → USB30_TX_CON_N1
FR3506 0R0402-PAD → USB30_TX_CON_P1
FC3505 SC1P50V2CN-1GP DY
FC3507 SC1P50V2CN-1GP DY

EU3501 PJE5UFN10A-GP

USB30_RX_CON_N1
USB30_RX_CON_P1
USB30_TX_CON_N1
USB30_TX_CON_P1

075.00510.0073
2nd = 075.00550.0071
3rd = 75.01045.073

5V_USB30_CHARGER
C3504 SC100U6D3V6MX-GP

ENG 0417 change

5V_USB30_CHARGER

USB1
VBUS, D-, D+, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, GND_DRAIN, GND
USB_CON_PN1
USB_CON_PP1
USB30_RX_CON_N1
USB30_RX_CON_P1
USB30_TX_CON_N1
USB30_TX_CON_P1
SKT-USB13-72-GP-U
22.10341.711
2nd = 22.10339.I41

PD 0624 change

<36> USB_CHAR_PP1
<36> USB_CHAR_PN1
EL3501 MCM1012B900FBP-GP-U
USB_CON_PP1
USB_CON_PN1
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

5V_USB30

USB2
VBUS, D-, D+, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, GND_DRAIN, GND
USB_CON_PN2
USB_CON_PP2
USB30_RX_CON_N2
USB30_RX_CON_P2
USB30_TX_CON_N2
USB30_TX_CON_P2
SKT-USB13-72-GP-U
22.10341.711
2nd = 22.10339.I41

PD 0624 change

<15> USB_PCH_PN2
<15> USB_PCH_PP2
EL3502 MCM1012B900FBP-GP-U
USB_CON_PN2
USB_CON_PP2
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001

EU3503 PJSRV05W-4DW6-GP

USB_CON_PN2
USB_CON_PP2
5V_S5
USB_CON_PN1
USB_CON_PP1

075.00005.0B7C
2nd = 075.01256.007C
3rd = 75.09904.07C

PD 0701 change

<18> USB30_RX_CPU_N2
<18> USB30_RX_CPU_P2
FR3508 0R0402-PAD → USB30_RX_CON_N2
FR3510 0R0402-PAD → USB30_RX_CON_P2
FC3509 SC1P50V2CN-1GP DY
FC3511 SC1P50V2CN-1GP DY

PD 0701 change

<18> USB30_TX_CPU_N2
<18> USB30_TX_CPU_P2
C3511 SCD1U16V2KX-L-GP
C3510 SCD1U16V2KX-L-GP
USB30_TX_N2_R
USB30_TX_P2_R
FR3512 0R0402-PAD → USB30_TX_CON_N2
FR3514 0R0402-PAD → USB30_TX_CON_P2
FC3513 SC1P50V2CN-1GP DY
FC3515 SC1P50V2CN-1GP DY

EU3502 PJE5UFN10A-GP

USB30_RX_CON_N2
USB30_RX_CON_P2
USB30_TX_CON_N2
USB30_TX_CON_P2

075.00510.0073
2nd = 075.00550.0071
3rd = 75.01045.073

<Core Design>

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Title: USB3.0 CONN

Size: A3 | Document Number: Newgate | Rev: 1M

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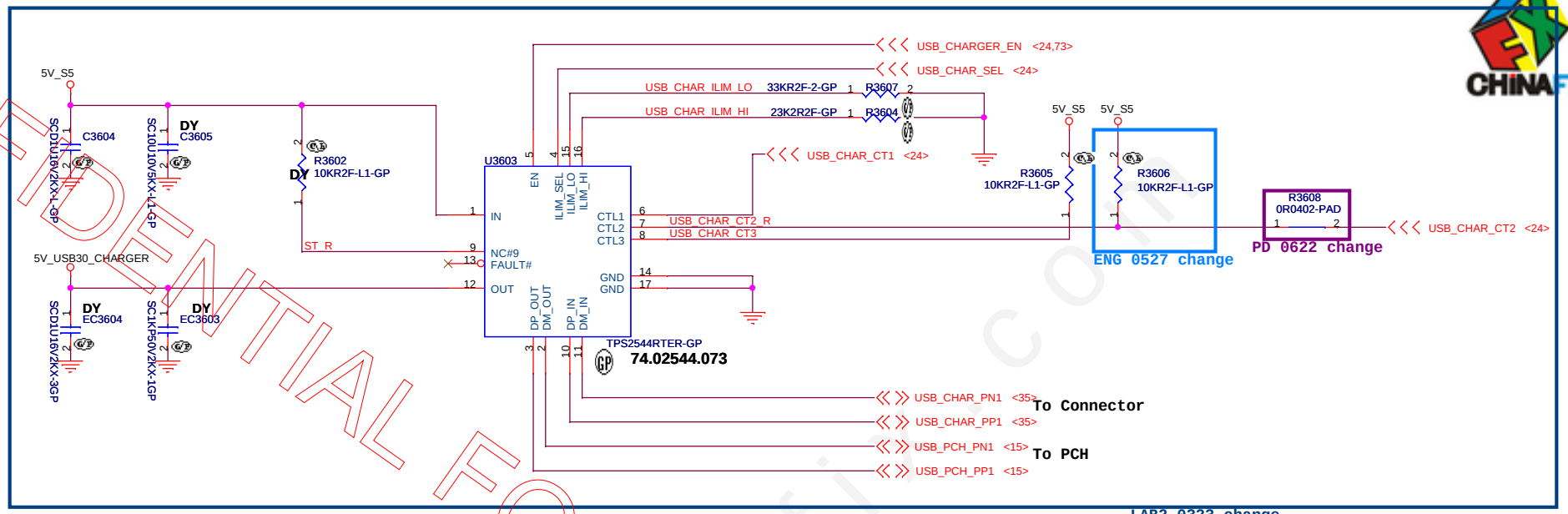

Table 2. Truth Table

CTL1	CTL2	CTL3	ILIM_ SEL	MODE	Current Limit Setting	Status Output	Notice
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data lines disconnected
0	0	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
0	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
0	1	0	1	SDP1	ILIM_HI	OFF	
0	1	1	0	DCP_Auto	ILIM_LO	OFF	Data lines disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP	Data lines disconnected Load Detect function active
1	0	0	0	DCP_Shorted	ILIM_LO	OFF	Device forced to stay in DCP BC1.2
1	0	0	1	DCP_Shorted	ILIM_HI	OFF	Charging mode
1	0	1	0	DCP/Divider1	ILIM_LO	OFF	Device forced to stay in DCP divider1
1	0	1	1	DCP/Divider1	ILIM_HI	OFF	Charging mode
1	1	0	0	SDP1	ILIM_LO	OFF	Data lines connected
1	1	0	1	SDP1	ILIM_HI	OFF	
1	1	1	0	SDP2	ILIM_LO	OFF	
1	1	1	1	CDP	ILIM_HI	CDP	Data lines disconnected Load Detect function active

<Core Design>

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Title: USB CHARGER

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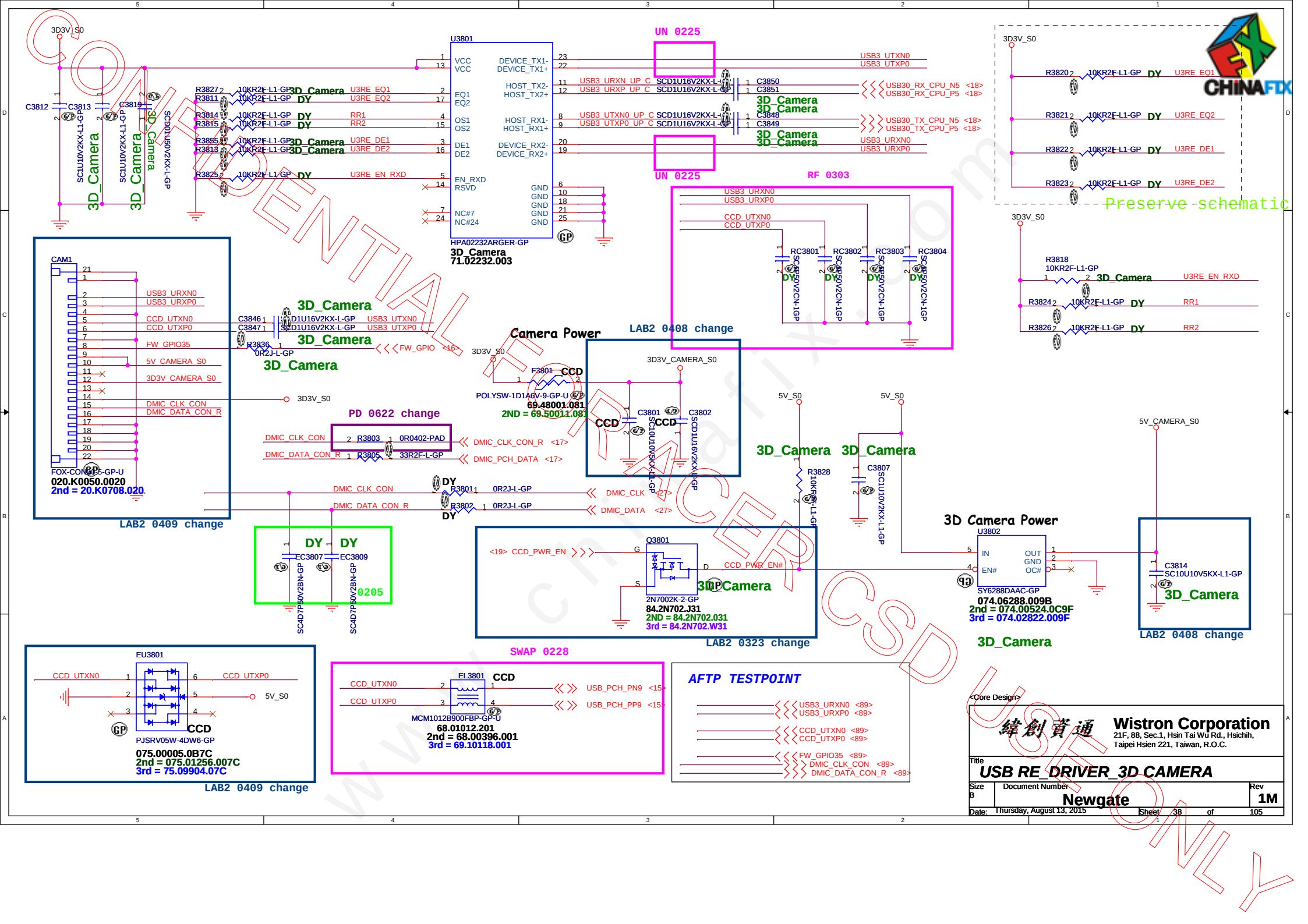
U3801
HPA02232ARGER-GP
3D_Camera
71.02232.003
UN 0225
UN 0225
RF 0303
CAM1
FOX-CONN-26-GP-U
020.K0050.0020
2nd = 20.K0708.020
LAB2 0409 change
Camera Power
LAB2 0408 change
POLYSW-1D1A6V-9-GP-U
69.48001.081
2ND = 69.50011.081
PD 0622 change
0R0402-PAD
33R2F-L-GP
0R2J-L-GP
DY
0205
SWAP 0228
MCM1012B900FBP-GP-U
68.01012.201
2nd = 68.00396.001
3rd = 69.10118.001
EU3801
PJSRV05W-4DW6-GP
075.00005.0B7C
2nd = 075.01256.007C
3rd = 75.09904.07C
LAB2 0409 change
Q3801
2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
3rd = 84.2N702.W31
LAB2 0323 change
3D Camera Power
SY6288DAAC-GP
074.06288.009B
2nd = 074.00524.0C9F
3rd = 074.02822.009F
LAB2 0408 change
AFTP TESTPOINT
Preserve schematic
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Power Sequence

PD 0622 change

<26,46> IMVP_PWRGD — R4002 0R0402-PAD — PCH_PWROK <17>

<17,24,53> PM_SLP_S3# — D4001 BAS16-X-GP

83.00016.I11
2nd = 83.00016.P11

LAB2 0323 change

<53> 1D5V_S0_PWRGD — R4017 0R0402-PAD — ALL_SYS_PWRGD <6,24>

PD 0622 change

C4020 SCD01U50V2KX-L-GP DY

R4018 0R0402-PAD — VR_EN <46>

PD 0622 change

ANNIE Run Power

<17,24,53> PM_SLP_S3# — R4001 0R0402-PAD — VTT_PWR

PD 0622 change

5V_S5 3D3V_S5

U4001 TPS22966DPUR-GP

VIN1#1 VIN1#2 ON1 VBIAS ON2 VIN2#6 VIN2#7
GND VOUT1#14 VOUT1#13 CT1 GND CT2 VOUT2#9 VOUT2#8

VTT_PWR
VTT_CT_3D3VC
VTT_CT_5VC
3D3V_S0
5V_S0

C4001 SCL1U07V2KX-L1-GP
C4002 SC221K50X-0MX-2GP
C4003 SCL1U07V2KX-L1-GP
C4004 SC2R2U10V5MX-GP DY
C4005 SC1U25V2KN-3GP DY
C4006 SC1U25V2KN-3GP DY
C4007 SCD1U16V2KX-L-GP
C4008 SCD1U16V2KX-L-GP

74.22966.093
2nd = 74.03523.A73
3rd = 074.05016.0093

LAB2 0323 change

<17,24,51> PM_SLP_S4# — R4008 0R0402-PAD
<17,24,53> PM_SLP_S3# — R4009 0R0402-PAD

PD 0622 change

1D2V_S3 1D0V_S5 5V_S5

PM_SLP_S4# R
PM_SLP_S3# R

U4002 TPS22966DPUR-GP

VIN1#1 VIN1#2 ON1 VBIAS ON2 VIN2#6 VIN2#7
GND VOUT1#14 VOUT1#13 CT1 GND CT2 VOUT2#9 VOUT2#8

VTT_CT_1V
VTT_CT_1D2V
1V_VCCST
1D2V_VCCSFR_OC

C4014 SCL1U07V2KX-L1-GP
C4015 SC1U06V3MX-1-GP DY
C4016 SCL1U07V2KX-L1-GP
C4017 SC1U06V3MX-1-GP DY
C4018 SC1U25V2KN-3GP DY
C4019 SC33P50V2JN-3GP DY

74.22966.093
2nd = 74.03523.A73
3rd = 074.05016.0093

PD 0622 change

<17,24,53> PM_SLP_S3# — R4006 0R0402-PAD — VCCSTG_EN_R

1D0V_S5 5V_S5

C4010 SCL1U07V2KX-L1-GP
C4009 SCL1U07V2KX-L1-GP
C4021 SCD01U50V2KX-L-GP DY

U4004 APE8939GN3-GP

VIN VIN VBIAS EN
VOUT#8 VOUT#7 VOUT#6 GND VIN

074.08939.0093

0D95V_VCCIO

C4012 SCD1U10V2KX-1-GP

LAB2 0323 change

LAB2 0323 change

<45> 3V_5V_EN — EC4001 SC2R2U10V5MX-GP DY — R4011 200KR2J-L1-GP DY

D4002 BAS16-4-GP

83.00016.I11
2nd = 83.00016.P11

PURE_HW_SHUTDOWN# <24,26>

R4012 2KR2F-L1-GP — S5_ENABLE <24,89>

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Title: Power Plane Enable & SEQUENCE

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12V_BT+_connector

PC4304
SCD1U25V2KX-L-GP

LAB2 0401 change

PN4302
SRN33J-7-GP-U

<24,44> BAT_IN#
<24,44> BAT_SCL
<24,44> BAT_SDA

BAT_IN# 1
BAT_SCL_1
BAT_SDA_1

BI

BAT1
ACES-CON10-38-GP-U2
20.F2133.010

PD 0627 change

PD3401
MMSZ5232BS-GP
83.5R603.Q3F
2ND = 83.5R603.K3F
3RD = 83.5R603.D3F
DY

PD4302
AZ5125-02S-R7G-GP
DY
75.05125.07D
2nd = 75.08212.07D

ENG 0428 change

Battery Reset

3D3V_RTC_AUX

PR4310
1MR2J-L-GP

BI_RST

RST1
SW-TACT-124-GP
62.40078.001
2nd = 62.40009.D71
3rd = 62.40089.441

3D3V_RTC_AUX

PR4309
10MR2J-L-GP
DY

BI

Q4301
DMN5L06K-7-GP

BI_RST

PR4307
0R2J-L-GP
DY

BIS

ENG 0417 change

Battery Insert

BIS

BTSW1
SW-TACT-5P-8-GP
62.40009.C91

PD 0624 change

AFTP TESTPOINT

<89> BI
<89> BAT_IN# 1
<89> BAT_SCL_1
<89> BAT_SDA_1

BI
BAT_IN# 1
BAT_SCL_1
BAT_SDA_1

ANNIE solution

Adaptor in to generate DCBATOUT

DCIN1
ACES-CONN12S-2-GP
20.F2434.006
2nd = 20.F2383.006

PD4301
P6SMBJ20A-GP
83.P6SMB.AAG
2nd = 083.00020.00AG

PC4302
SC1U50V5ZY-1-GP-U

AD_JK

PC4305
SCD1U50V3KX-L-GP

LAB2 0323 change

<24> AD_OFF

PQ4304
LTC024EUB-K8-GP
84.00024.A1K
2ND = 84.00124.H1K
3rd = 84.00124.V1K

PWR_ADJK_EN

PQ4305
LTA024EUB-FS8-GP
84.00024.01K
2nd = 84.02303.01K

ENG 0428 change

AD_JK

PR4305
200KR3F-GP

PC4306
SC1U50V5ZY-1-GP-U

PWR_AD+_2

PR4304
100KR2F-L3-GP

19V_AD+

PU4302
TPCC8103-GP
84.08103.037
2nd = 084.03335.0037

ENG 0428 change

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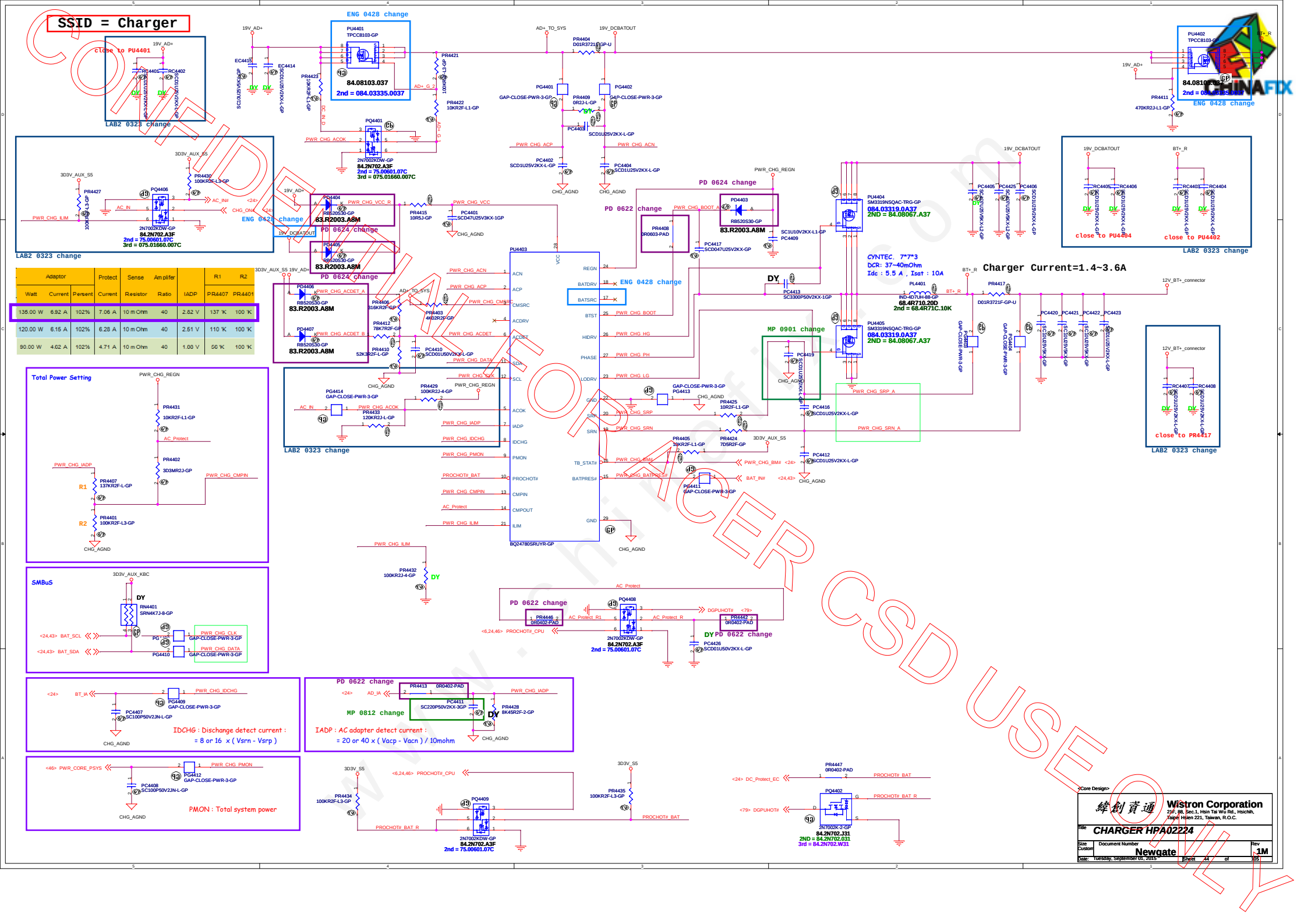

Adaptor			Protect	Sense	Amplifer		R1	R2
Watt	Current	Persent	Current	Resistor	Ratio	IADP	PR4407	PR4401
135.00 W	6.92 A	102%	7.06 A	10 m Ohm	40	2.82 V	137 K	100 K
120.00 W	6.15 A	102%	6.28 A	10 m Ohm	40	2.51 V	110 K	100 K
90.00 W	4.62 A	102%	4.71 A	10 m Ohm	40	1.00 V	50 K	100 K

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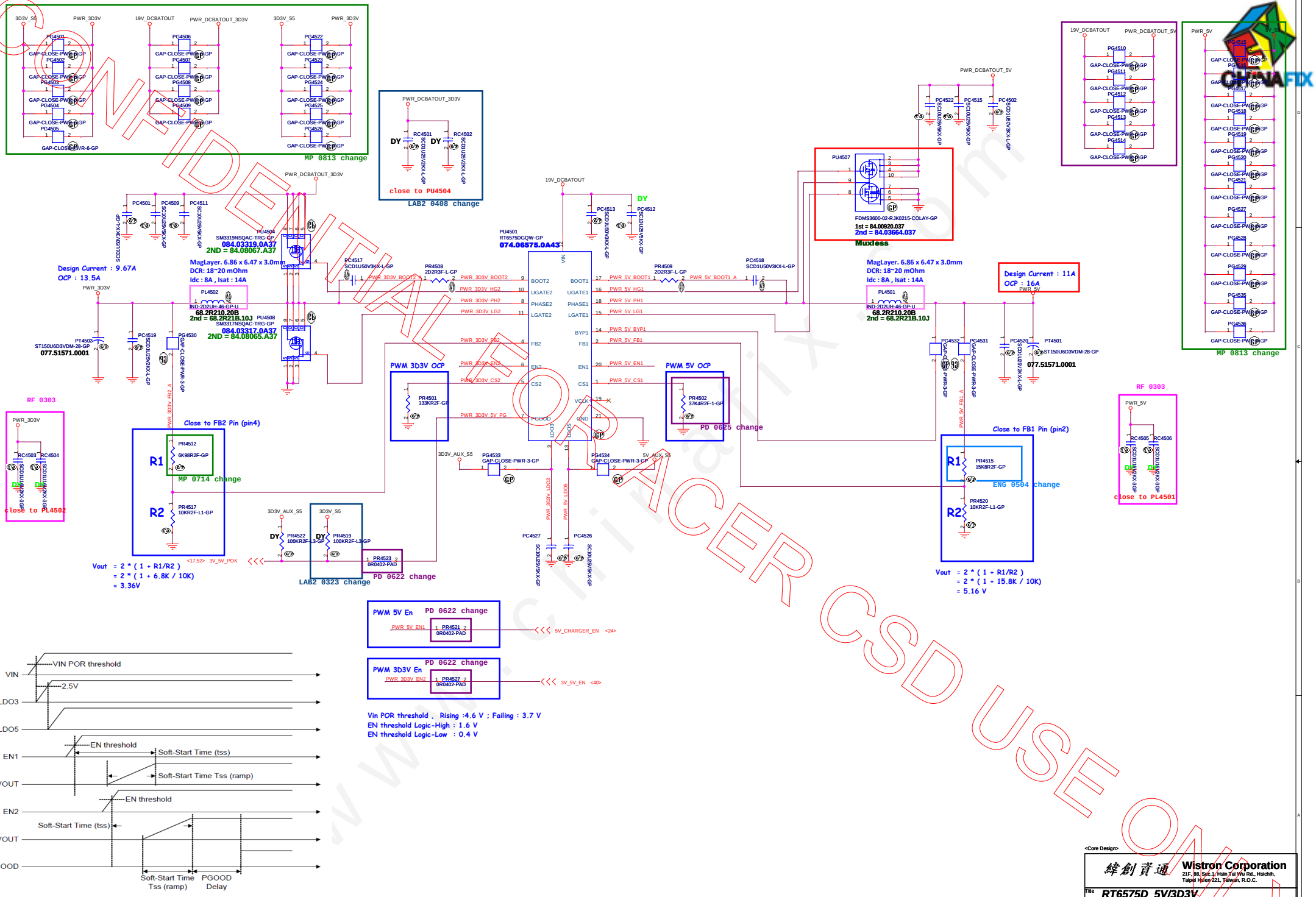

Figure 6. RT6575B Timing

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Title: RT6575D_5V/3D3V
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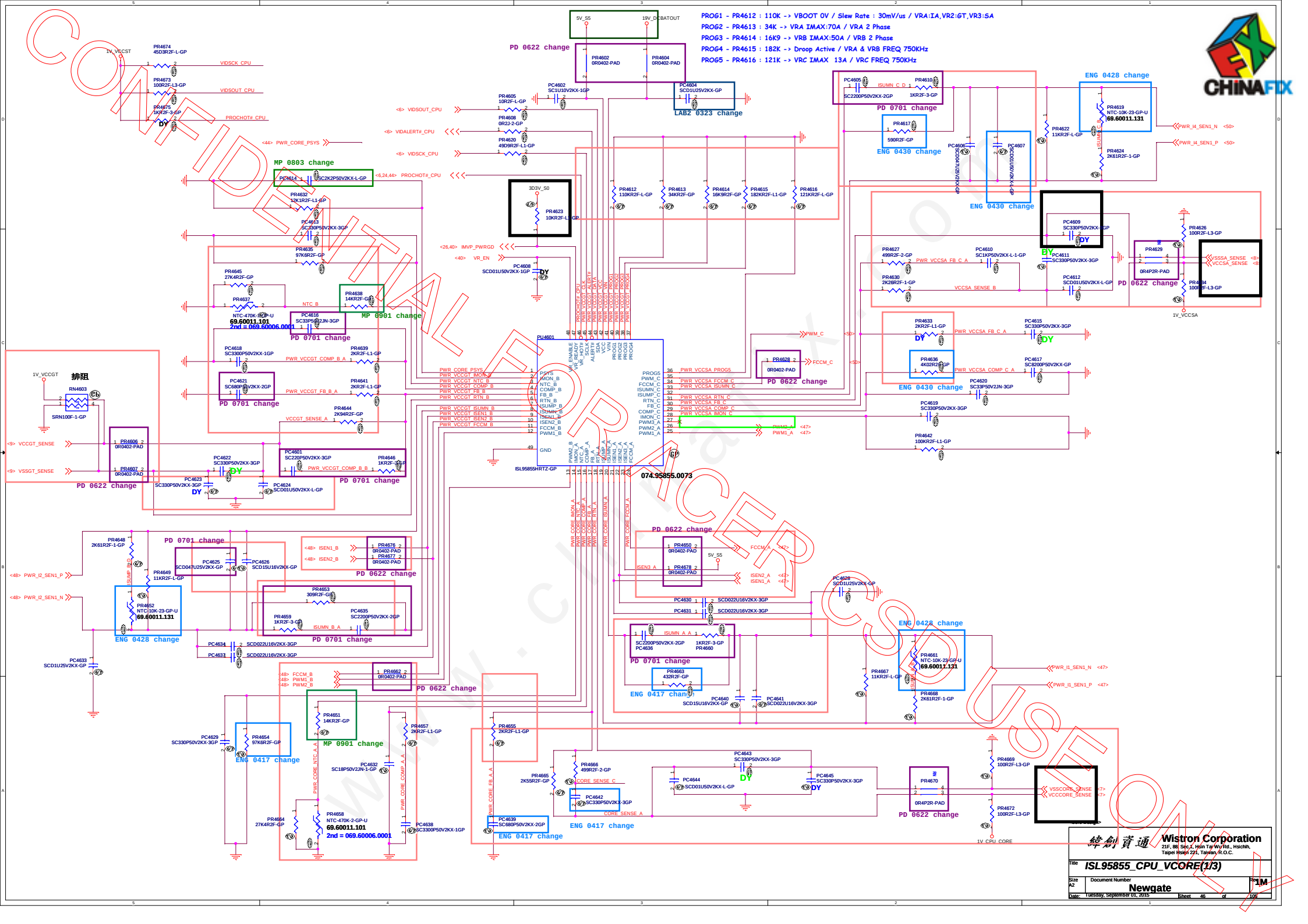
PROG1 - PR4612 : 110K -> VBOOT 0V / Slew Rate : 30mV/us / VRA:IA,VR2:GT,VR3:SA
PROG2 - PR4613 : 34K -> VRA IMAX:70A / VRA 2 Phase
PROG3 - PR4614 : 16K9 -> VRB IMAX:50A / VRB 2 Phase
PROG4 - PR4615 : 182K -> Droop Active / VRA & VRB FREQ 750KHz
PROG5 - PR4616 : 121K -> VRC IMAX 13A / VRC FREQ 750KHz
PD 0622 change
LAB2 0323 change
PD 0701 change
ENG 0428 change
ENG 0430 change
MP 0803 change
MP 0901 change
ENG 0417 change
DY
ISL95855HRTZ-GP
074.95855.0073
1V_VCCSA
1V_CPU_CORE
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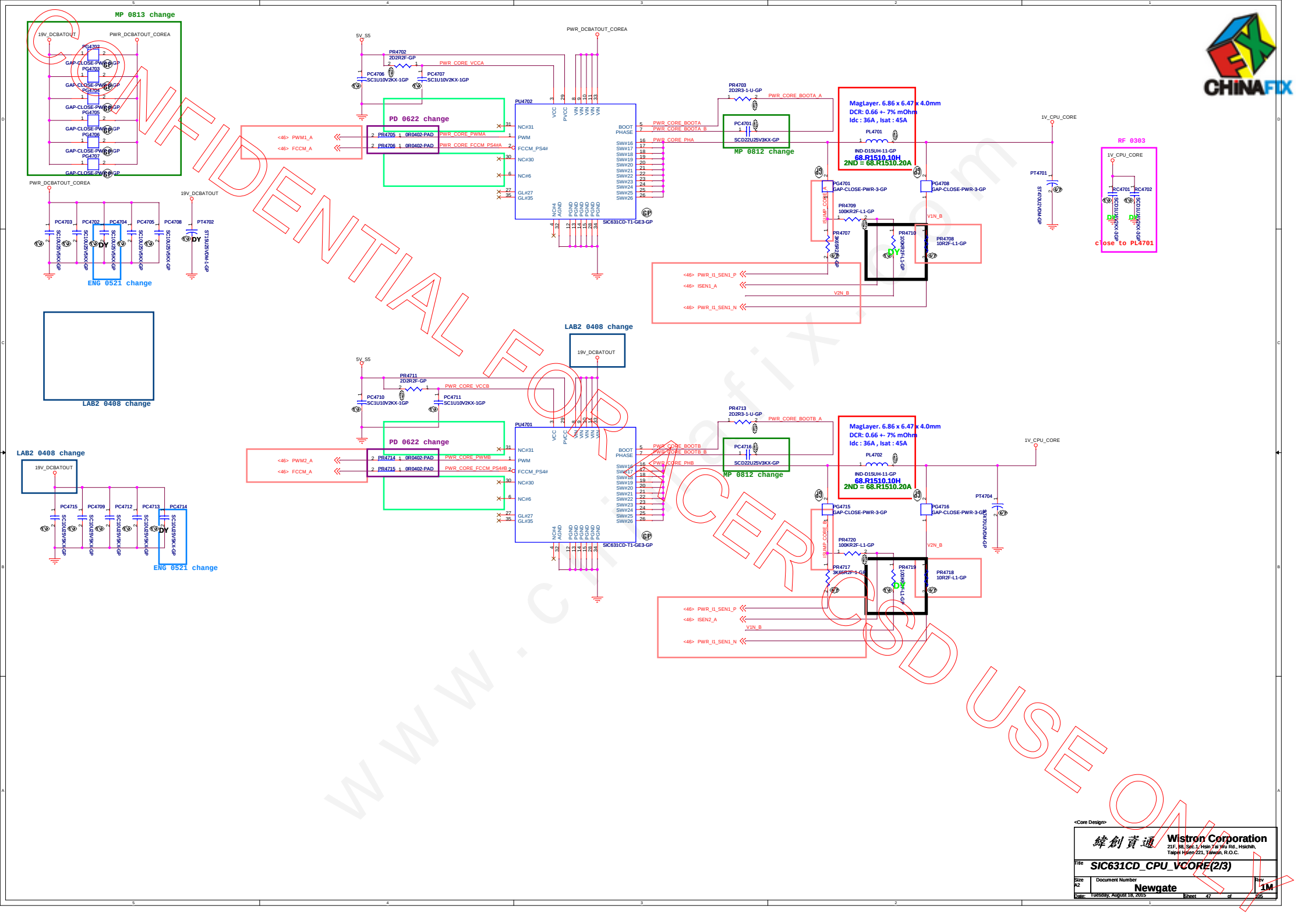
MP 0813 change
19V_DCBATOUT
PWR_DCBATOUT_COREA
PC4702
PC4703
PC4704
PC4705
PC4706
PC4707
GAP-CLOSE-PWR-3-GP
PWR_DCBATOUT_COREA
19V_DCBATOUT
PC4703
PC4702
PC4704
PC4705
PC4708
PT4702
SC1U25V5KX-GP
ST15U25VDM1-GP
DY
ENG 0521 change
LAB2 0408 change
5V_S5
PR4702
2D2R2F-GP
PWR_CORE_VCCA
PC4706
SC1U10V2KX-1GP
PC4707
SC1U10V2KX-1GP
PD 0622 change
<46> PWM1_A
<46> FCCM_A
PR4705
PR4706
0R0402-PAD
PWR_CORE_PWMA
PWR_CORE_FCCM_PS4#A
PU4702
NC#31
PWM
FCCM_PS4#
NC#30
NC#6
GL#27
GL#35
VCC
PVCC
VIN
BOOT
PHASE
SW#16
SW#17
SW#18
SW#19
SW#20
SW#21
SW#22
SW#23
SW#24
SW#25
SW#26
NC#4
AGND
PGND
SIC631CD-T1-GE3-GP
PWR_DCBATOUT_COREA
PR4703
2D2R3-1-U-GP
PWR_CORE_BOOTA_A
PC4701
SCD22U25V3KX-GP
MP 0812 change
PWR_CORE_BOOTA
PWR_CORE_BOOTA_B
PWR_CORE_PHA
MagLayer. 6.86 x 6.47 x 4.0mm
DCR: 0.66 +- 7% mOhm
Idc : 36A , Isat : 45A
PL4701
IND-D15UH-11-GP
68.R1510.10H
2ND = 68.R1510.20A
PG4701
GAP-CLOSE-PWR-3-GP
PG4708
GAP-CLOSE-PWR-3-GP
ISUM-
ISUM+
PR4709
100K2F-L1-GP
PR4707
3K65R2F-GP
PR4710
10R2F-L1-GP
PR4708
10R2F-L1-GP
V1N_B
V2N_B
<46> PWR_I1_SEN1_P
<46> ISEN1_A
<46> PWR_I1_SEN1_N
1V_CPU_CORE
PT4701
ST470U2VDM-GP
RF 0303
RC4701
RC4702
SC10U10V3KX-GP
close to PL4701
LAB2 0408 change
19V_DCBATOUT
PC4715
PC4709
PC4712
PC4713
PC4714
SC10U25V5KX-GP
DY
ENG 0521 change
LAB2 0408 change
5V_S5
PR4711
2D2R2F-GP
PWR_CORE_VCCB
PC4710
SC1U10V2KX-1GP
PC4711
SC1U10V2KX-1GP
PD 0622 change
<46> PWM2_A
<46> FCCM_A
PR4714
PR4715
0R0402-PAD
PWR_CORE_PWMB
PWR_CORE_FCCM_PS4#B
PU4701
NC#31
PWM
FCCM_PS4#
NC#30
NC#6
GL#27
GL#35
VCC
PVCC
VIN
BOOT
PHASE
SW#16
SW#17
SW#18
SW#19
SW#20
SW#21
SW#22
SW#23
SW#24
SW#25
SW#26
NC#4
AGND
PGND
SIC631CD-T1-GE3-GP
LAB2 0408 change
19V_DCBATOUT
PR4713
2D2R3-1-U-GP
PWR_CORE_BOOTB_A
PC4716
SCD22U25V3KX-GP
MP 0812 change
PWR_CORE_BOOTB
PWR_CORE_BOOTB_B
PWR_CORE_PHB
MagLayer. 6.86 x 6.47 x 4.0mm
DCR: 0.66 +- 7% mOhm
Idc : 36A , Isat : 45A
PL4702
IND-D15UH-11-GP
68.R1510.10H
2ND = 68.R1510.20A
PG4715
GAP-CLOSE-PWR-3-GP
PG4716
GAP-CLOSE-PWR-3-GP
ISUM-
ISUM+
PR4720
100K2F-L1-GP
PR4717
3K65R2F-GP
PR4719
10R2F-L1-GP
PR4718
10R2F-L1-GP
V2N_B
V1N_B
<46> PWR_I1_SEN1_P
<46> ISEN2_A
<46> PWR_I1_SEN1_N
1V_CPU_CORE
PT4704
470U2VDM-GP
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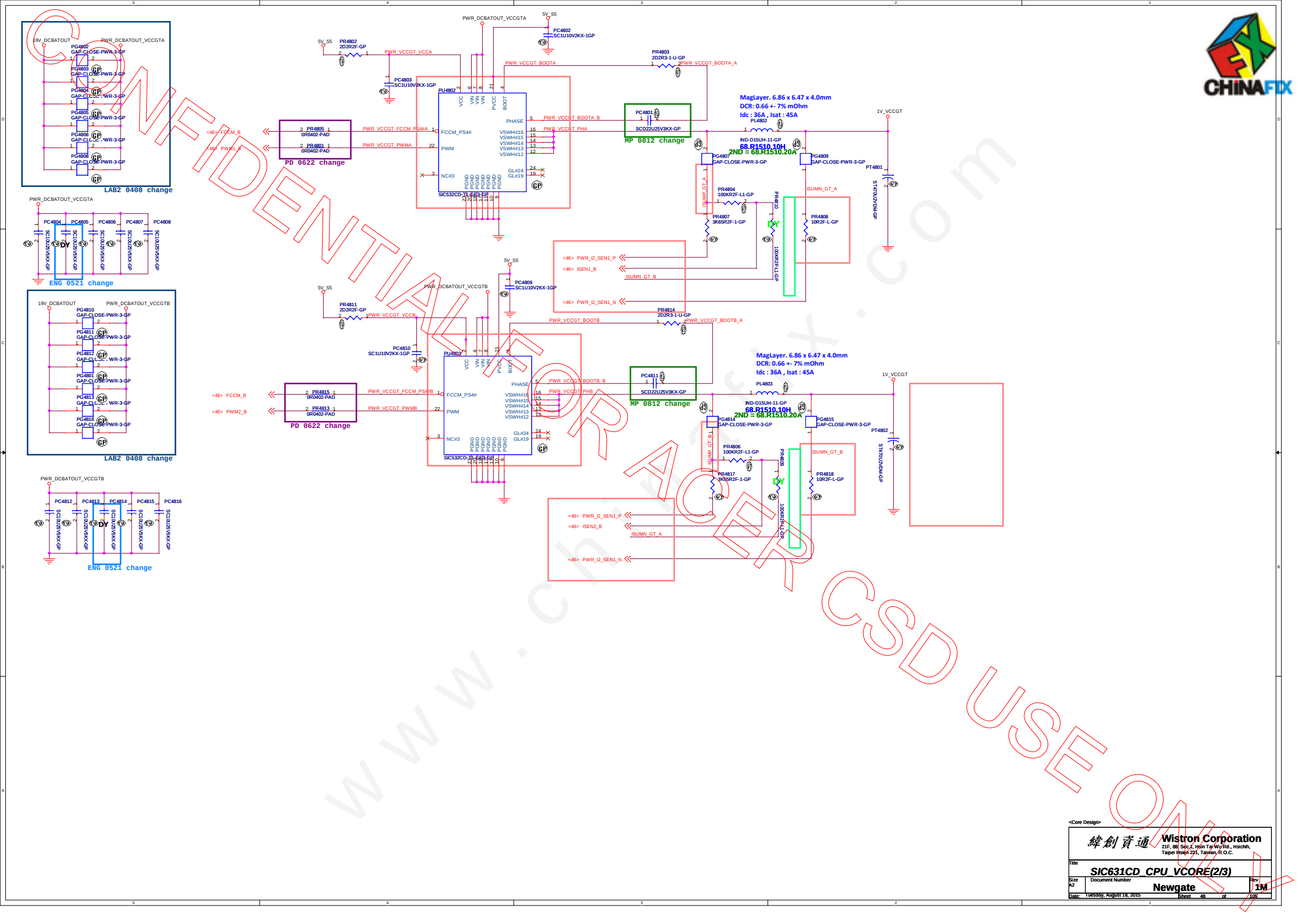

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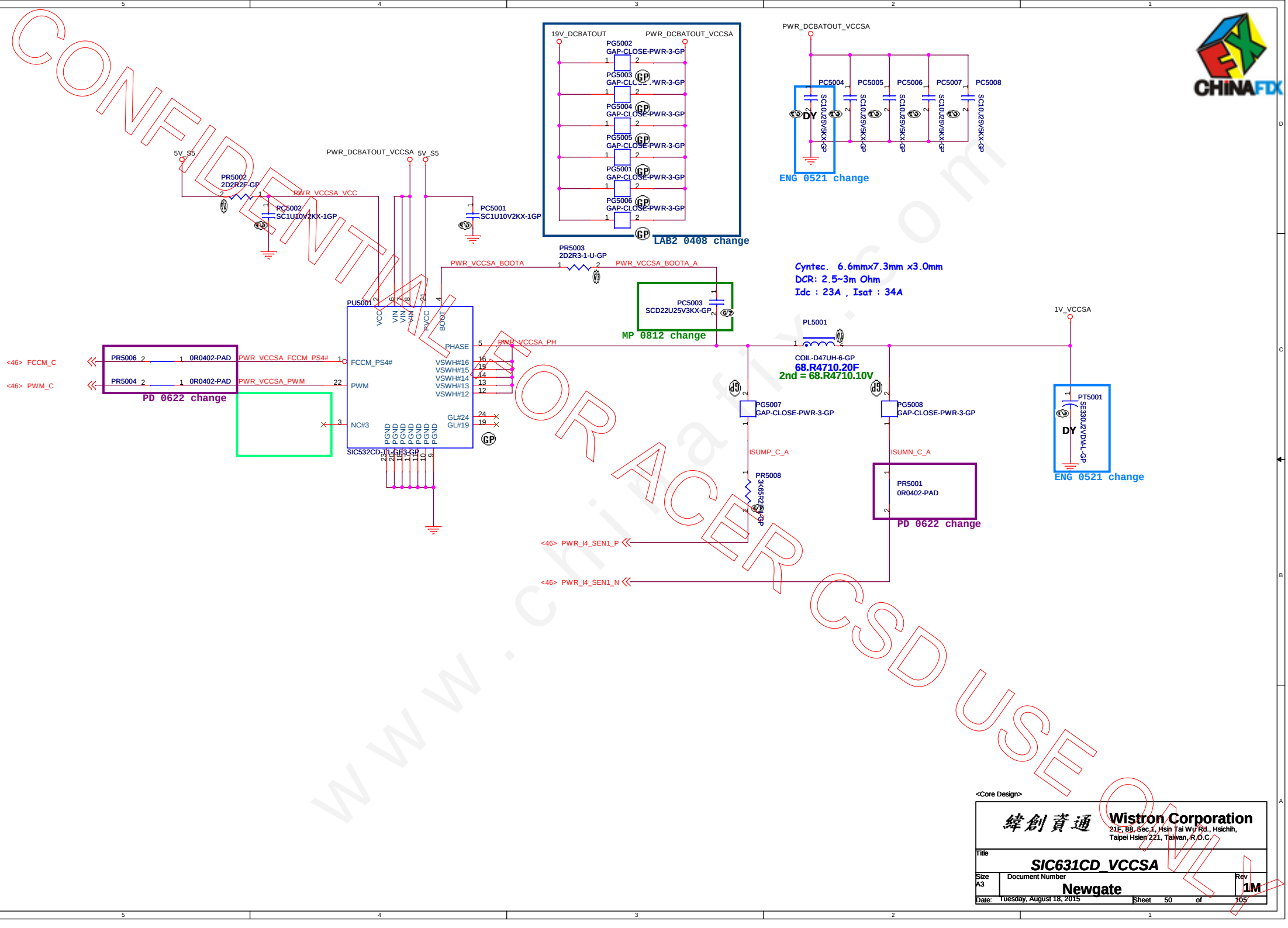

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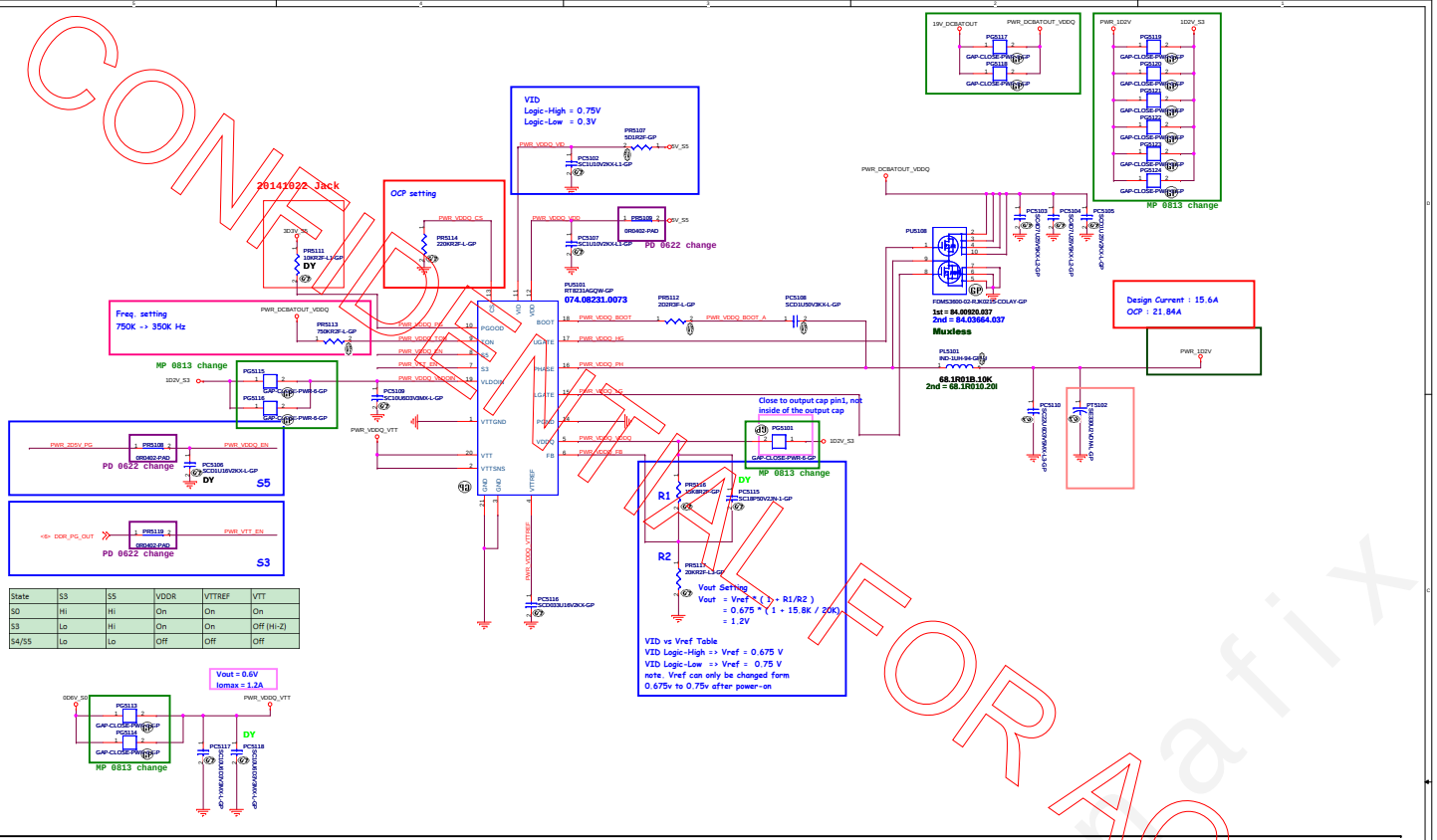
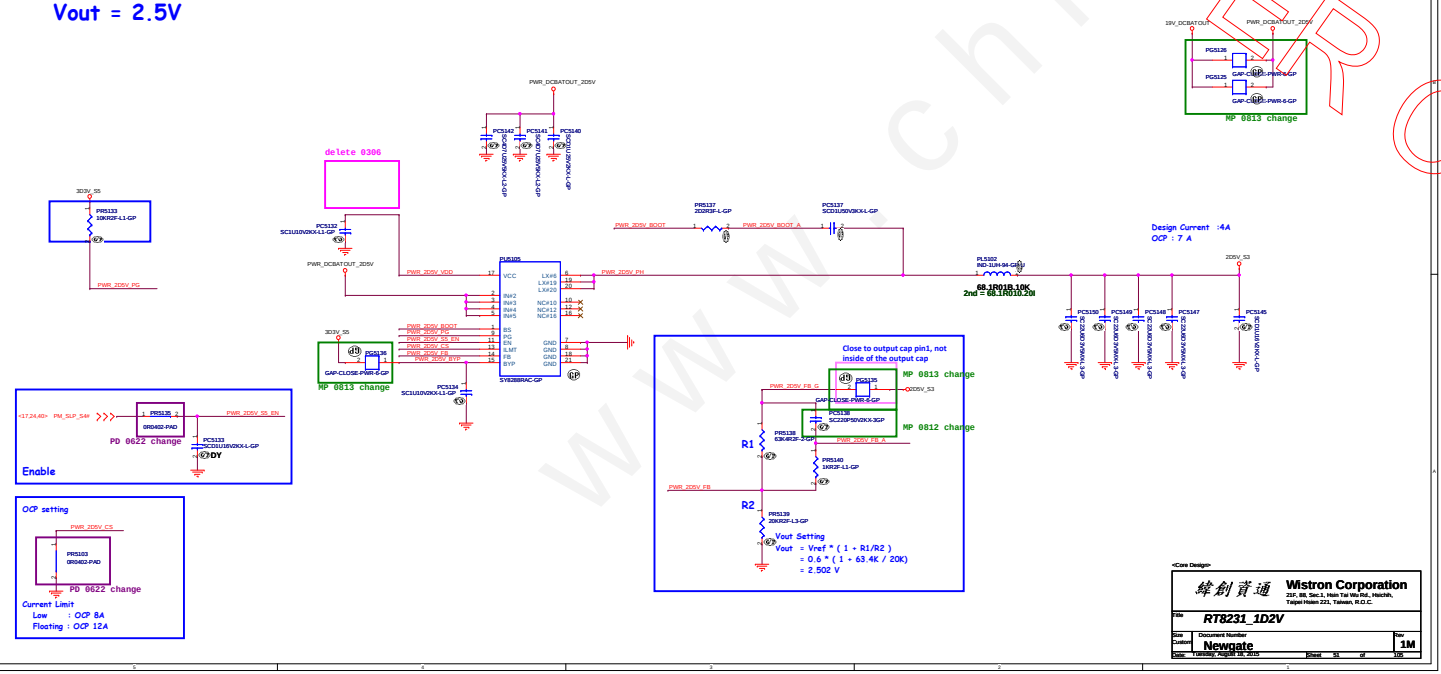


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

SY8288 For DDR4
Vout = 2.5V



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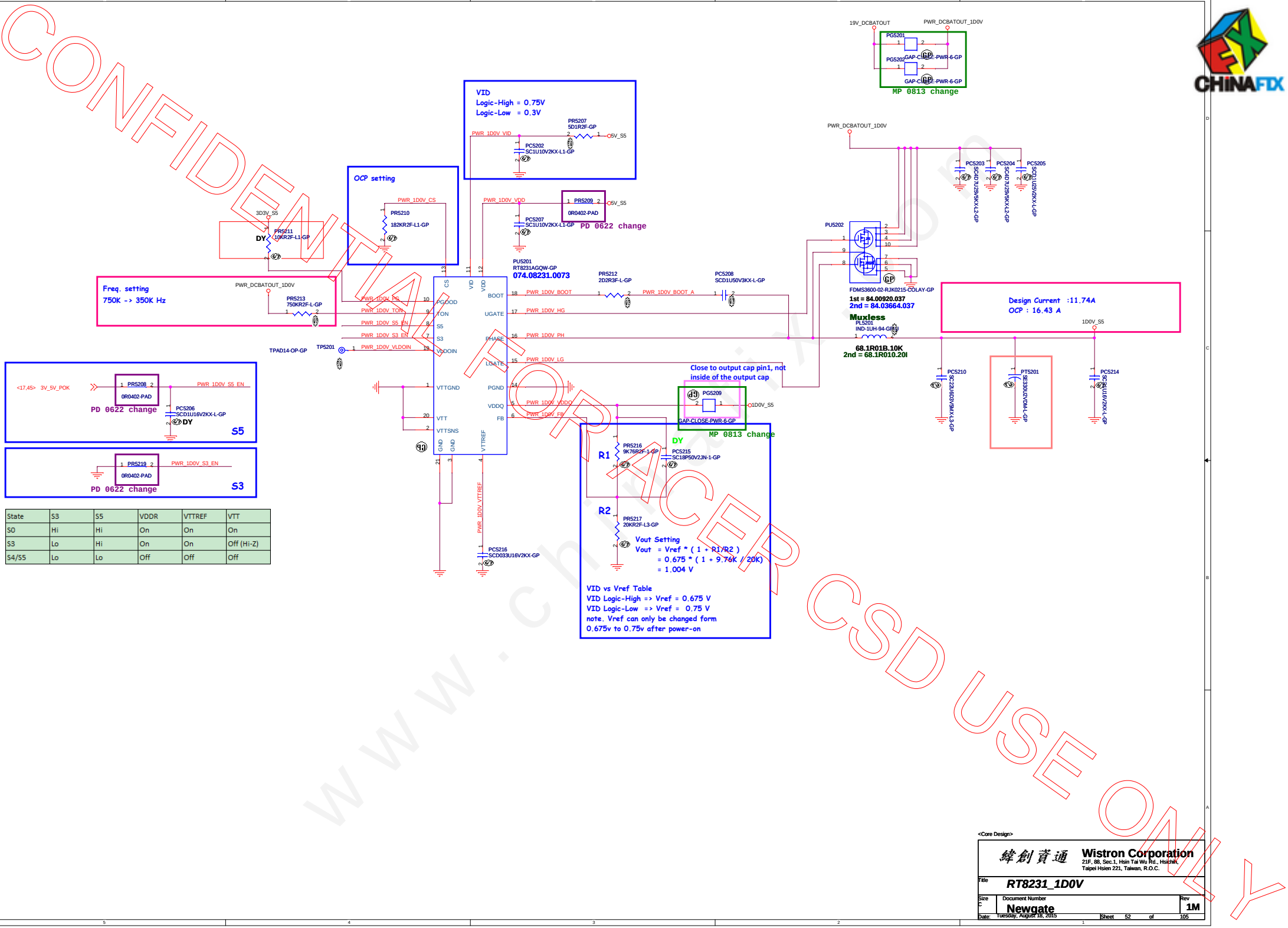

State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

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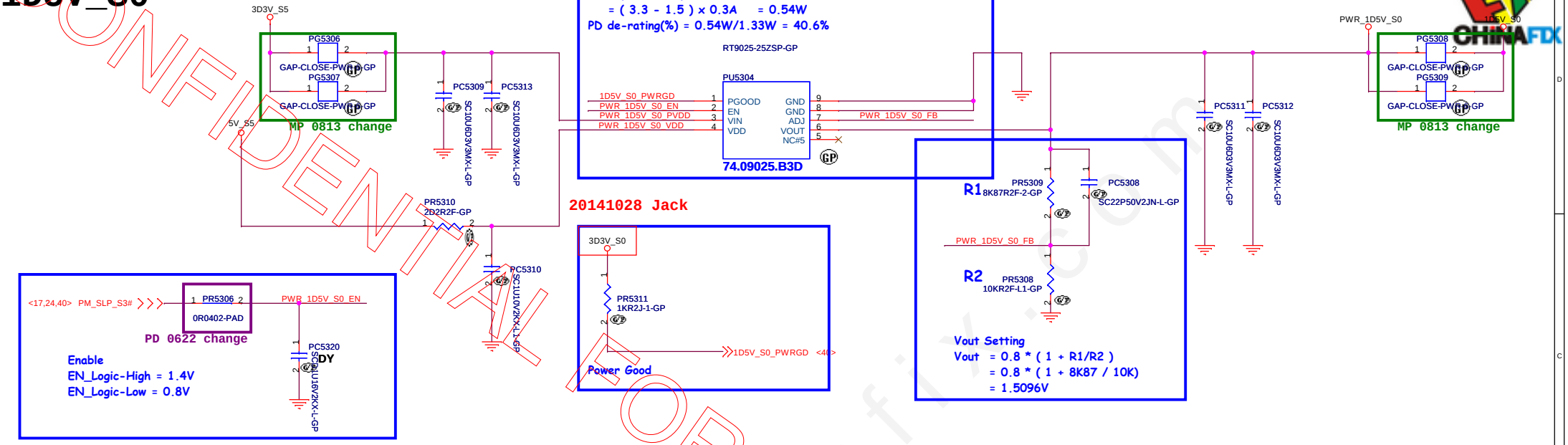
1D5V_S0



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Title	RT9025_1D5V	
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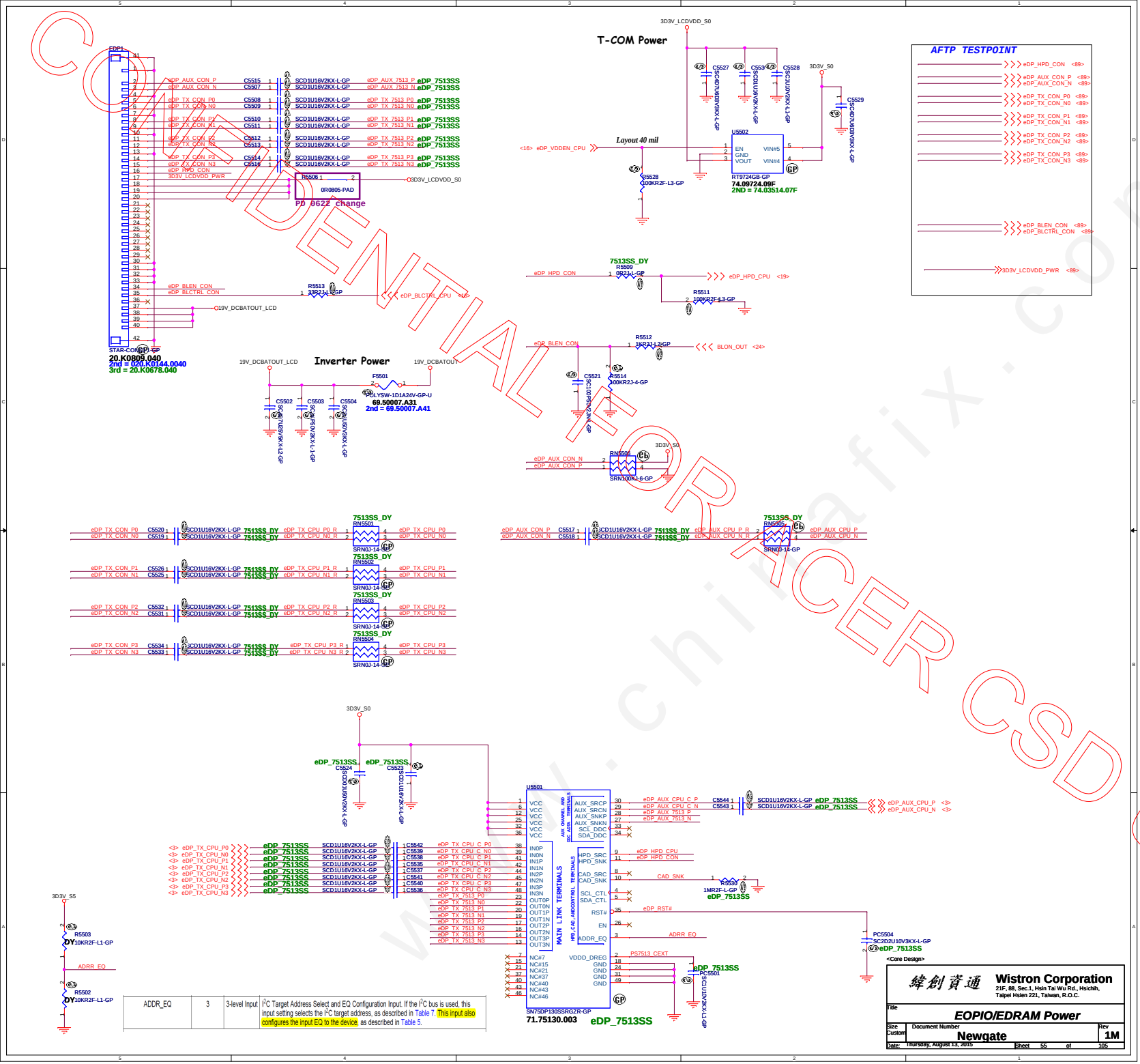
Size	Document Number	Rev
A	**Newgate**	**1M**

Date: Wednesday, August 12, 2015 Sheet 54 of 105



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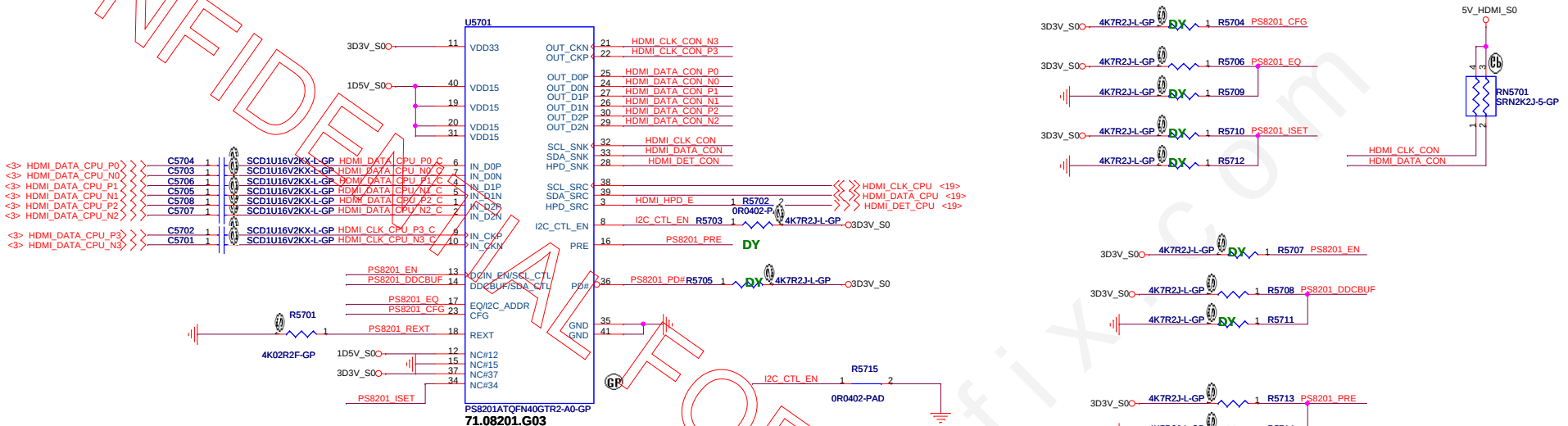
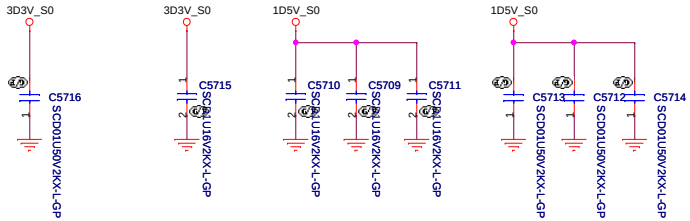
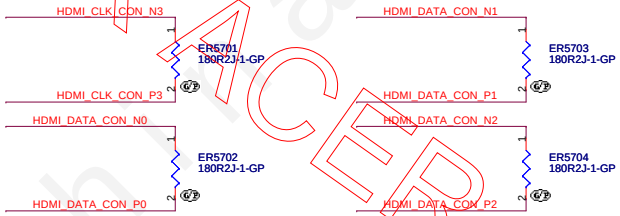
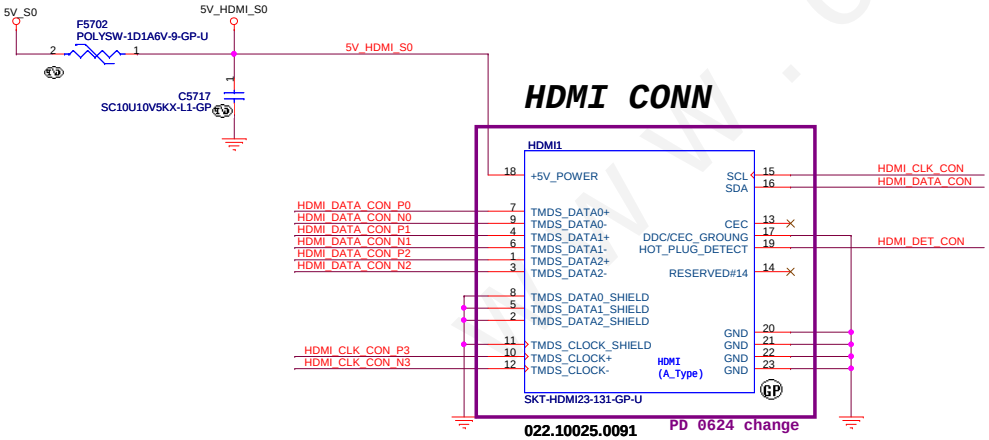
SSID = VIDEO

HDMI Level Shifter & CONNECTOR









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Title: HDMI Level Shifter/Conn

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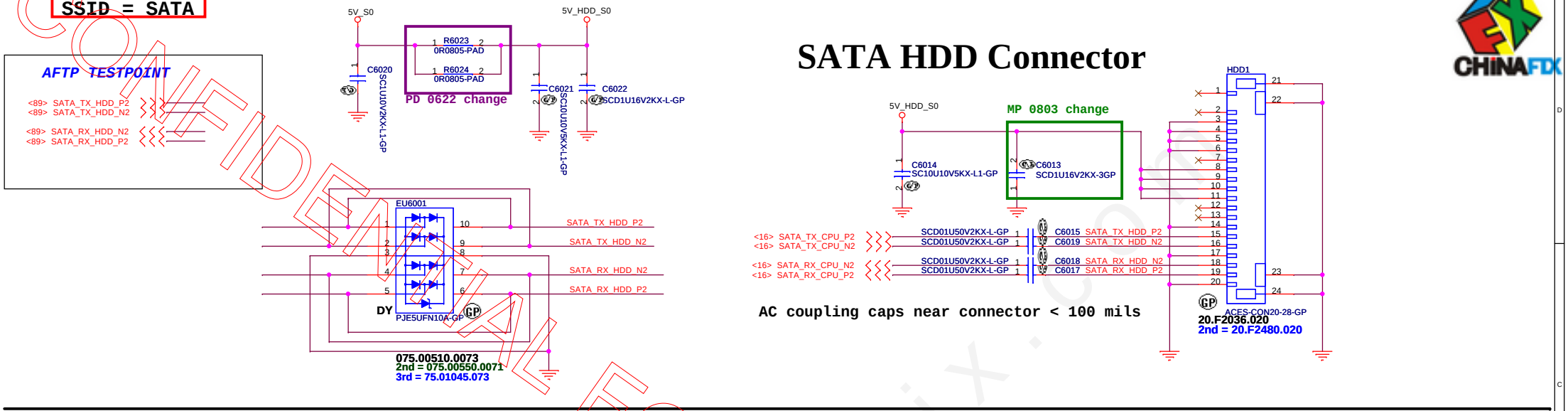
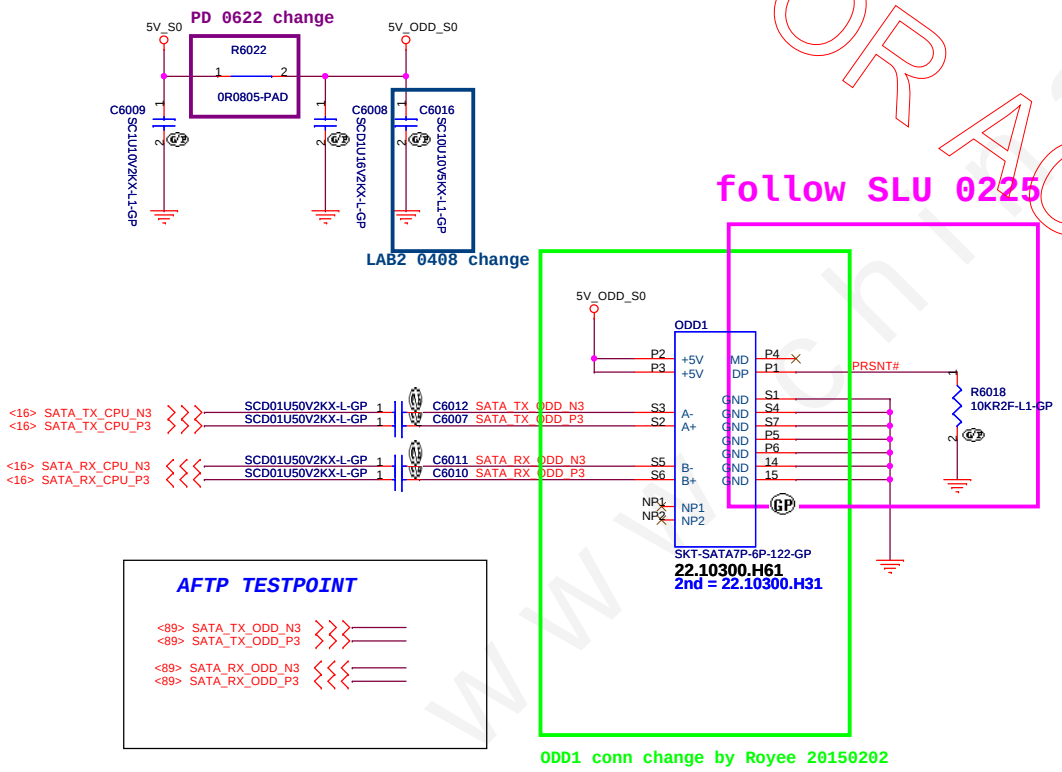
SSID = SATA

SATA HDD Connector





PIN DEFINE	CONN	FFC
GND	P5/P6	20
GND		19
GND		18
ODD_DA	P4	17
NC		16
5V	P2/P3	15
5V		14
5V		13
5V		12
5V		11
5V		10
NC		9
PRSNT	P1	8
GND	S7	7
RXP	S6	6
RXN	S5	5
GND	S4	4
TXN	S3	3
TXP	S2	2
GND	S1	1

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Title: HDD/ODD

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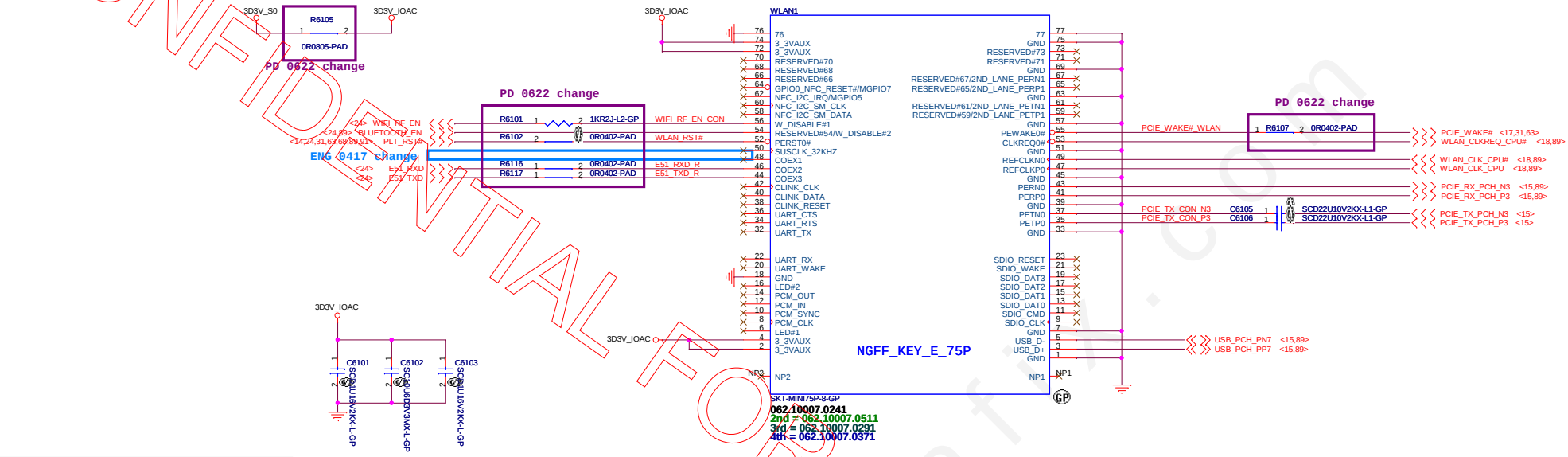
SSID = Wireless/ Wigig

NGFF Connector (802.11a/b/g/n)



AFTP TESTPOINT

PCIE_WAKE#_WLAN <89>
WLAN_CLKREQ_CPU# <18,89>
WLAN_CLK_CPU# <18,89>
WLAN_CLK_CPU <18,89>
PCIE_RX_PCH_N3 <15,89>
PCIE_RX_PCH_P3 <15,89>
PCIE_TX_CON_N3 <89>
PCIE_TX_CON_P3 <89>
USB_PCH_PN7 <15,89>
USB_PCH_PP7 <15,89>
WIFI_RF_EN_CON <89>
BLUETOOTH_EN <24,89>
WLAN_RST# <89>
ENG 0417 change
E51_RXD_R <89>
E51_TXD_R <89>

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Title: Mini card-WLAN

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SSID = Wireless

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Mini Card Connector (NGFF m-SATA)

SSID = m-SATA

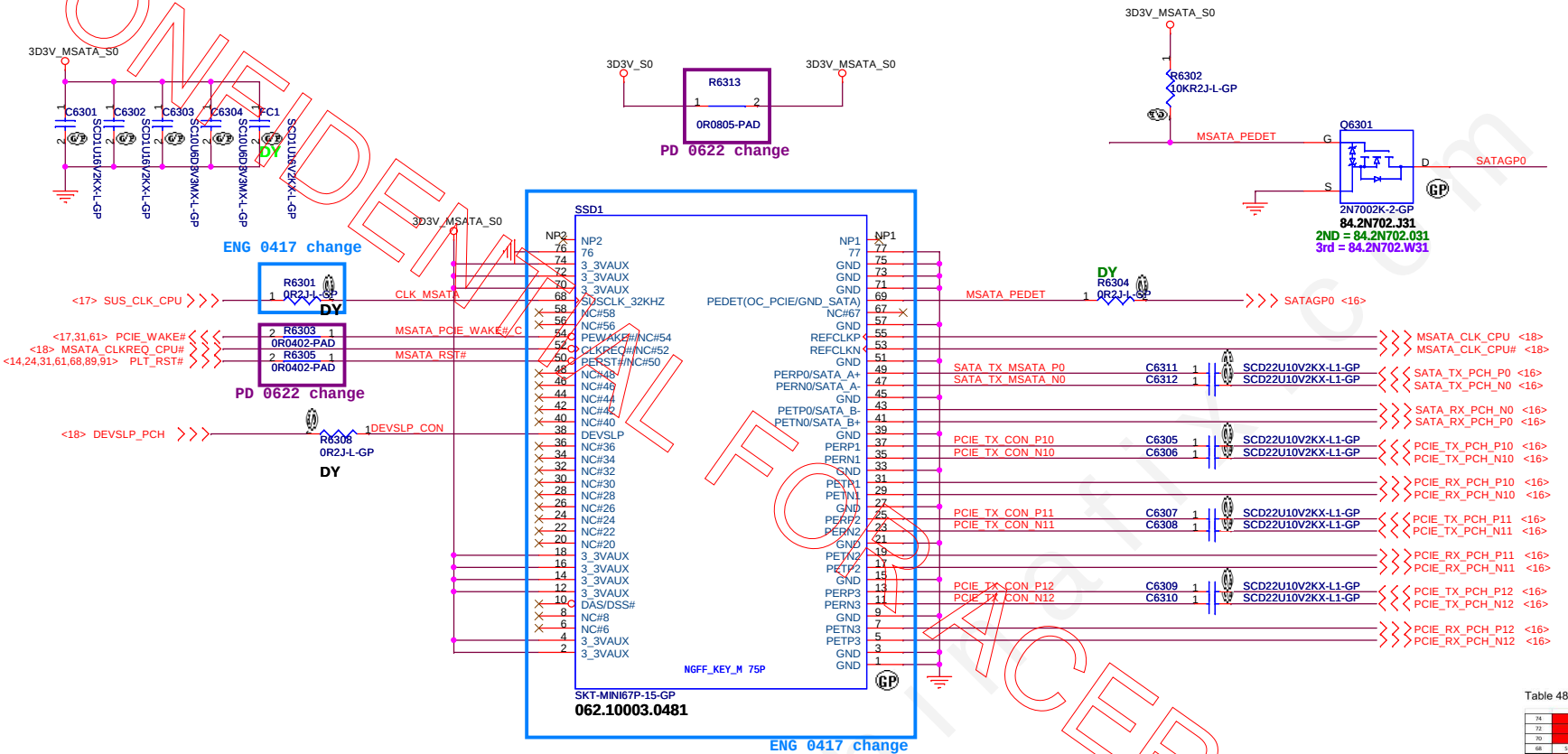

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

Table 34-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.

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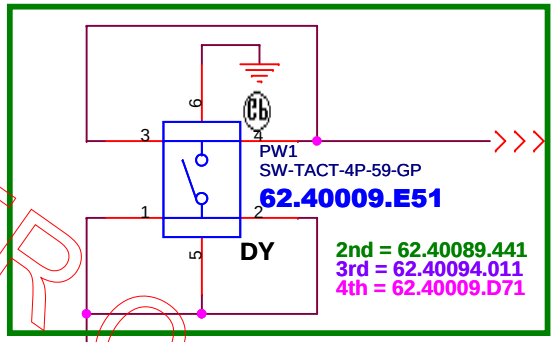
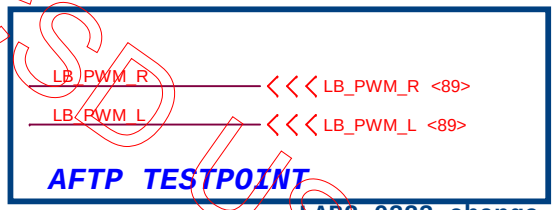
SSID = User.Interface

LAB2 0401 change

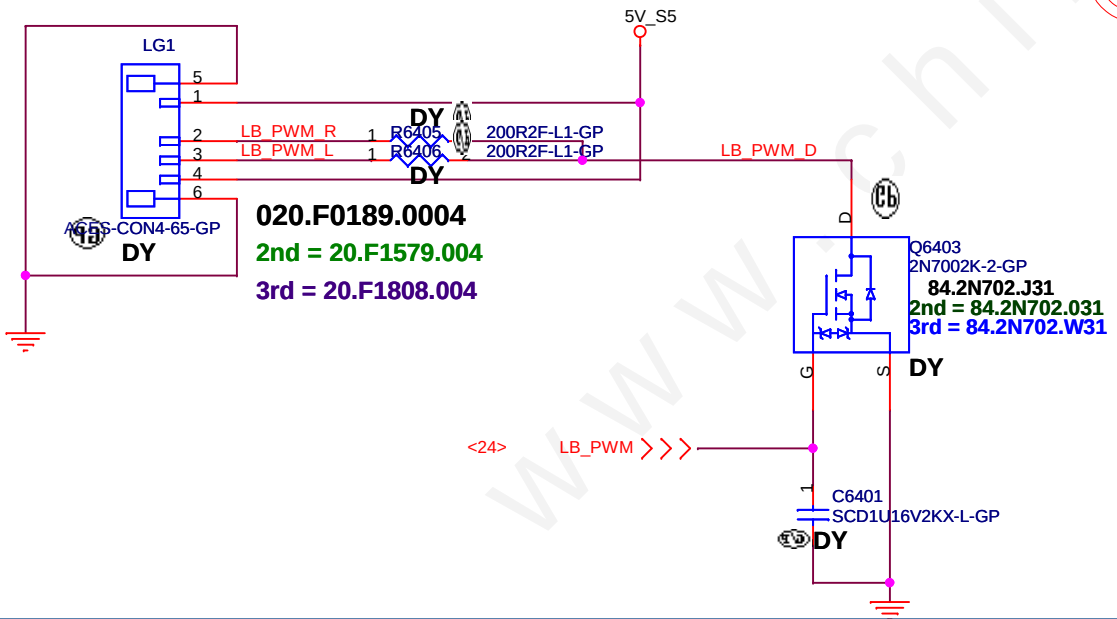
Power Button



MP 0730 change



LAB2 0323 change



LAB2 0323 change

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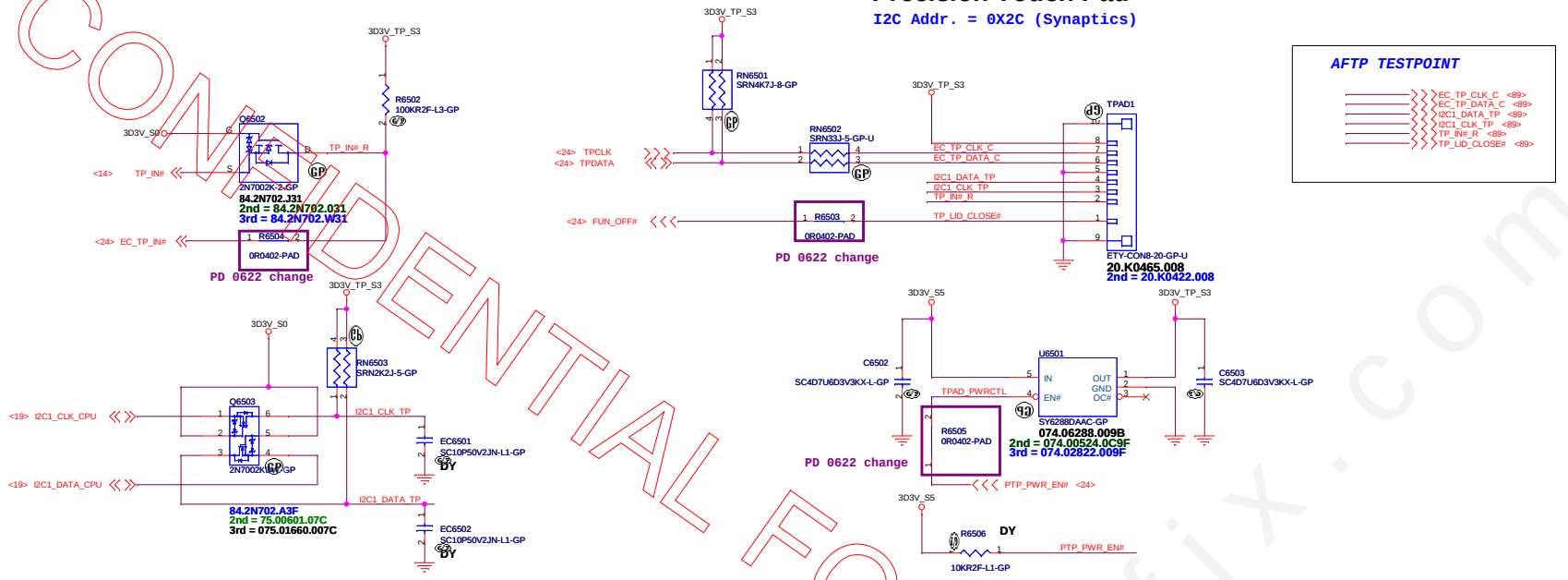
Precision Touch Pad

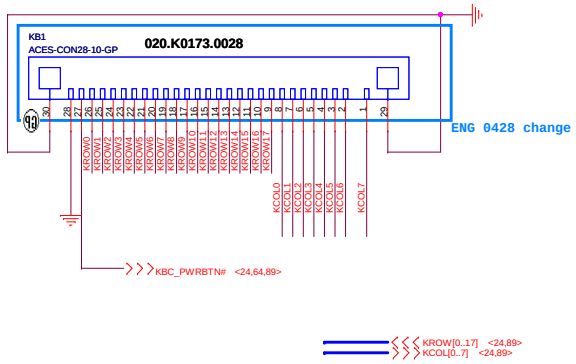
I2C Addr. = 0X2C (Synaptics)



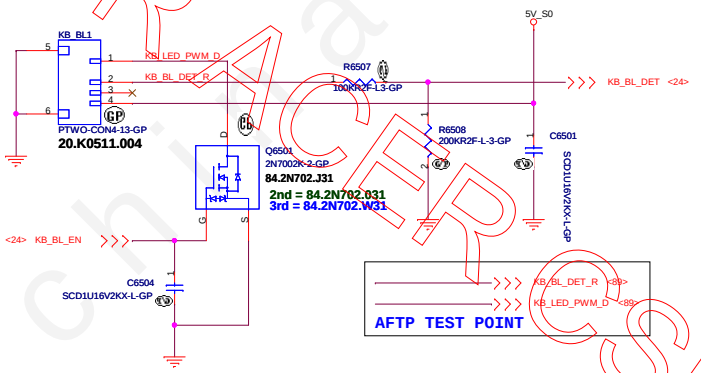
AFTP TESTPOINT

EC_TP_CLK_C <89>
EC_TP_DATA_C <89>
I2C1_DATA_TP <89>
I2C1_CLK_TP <89>
TP_IN#_R <89>
TP_LID_CLOSE# <89>

Internal KeyBoard Connector

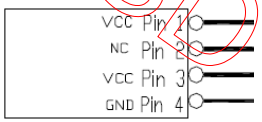


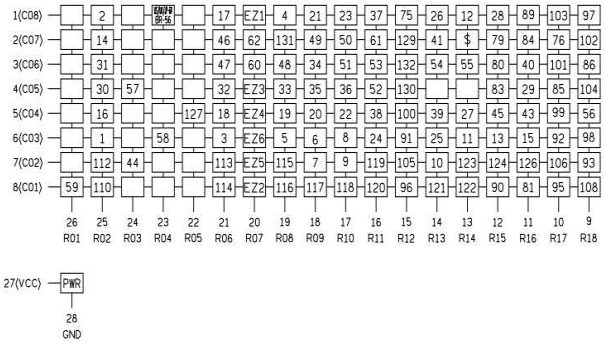
KROW[0..17] <24,89>
KCOL[0..7] <24,89>



AFTP TEST POINT

KB_BL_DET_R <89>
KB_LED_PWM_D <89>





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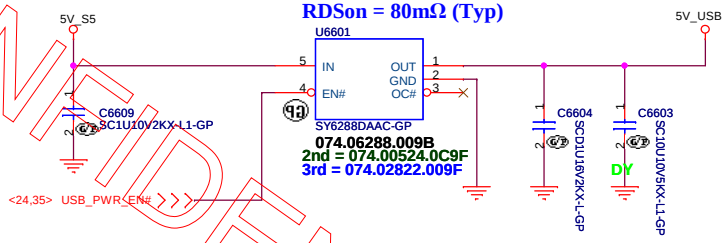
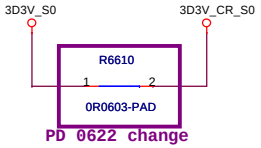
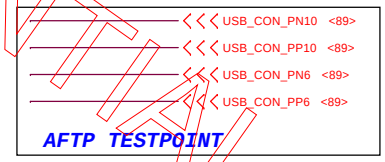
Low Active 2A
RDSon = 80mΩ (Typ)

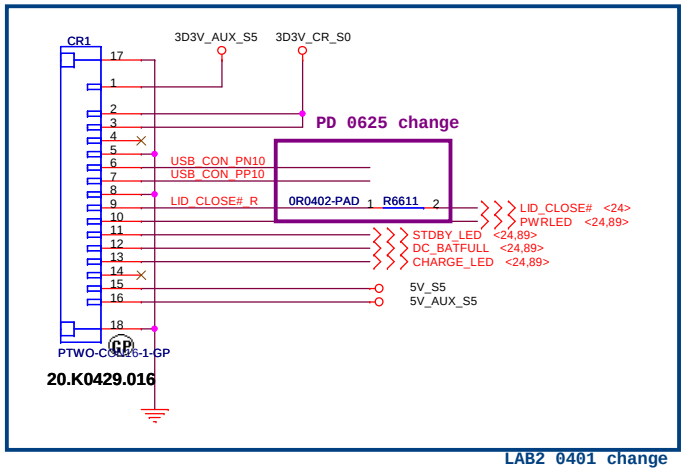




PD 0622 change

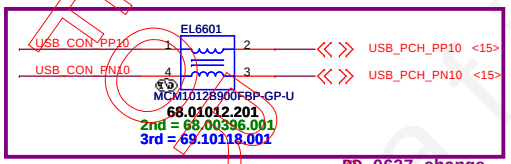


Card Reader

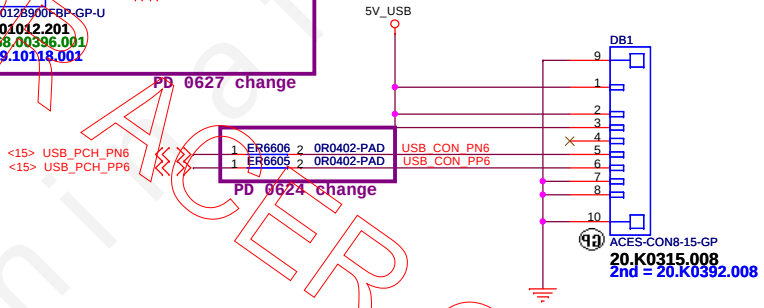


LAB2 0401 change

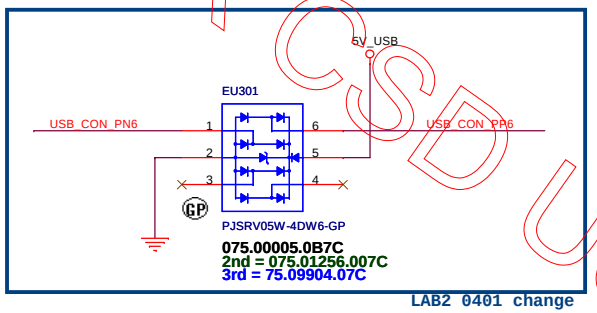
USB2.0



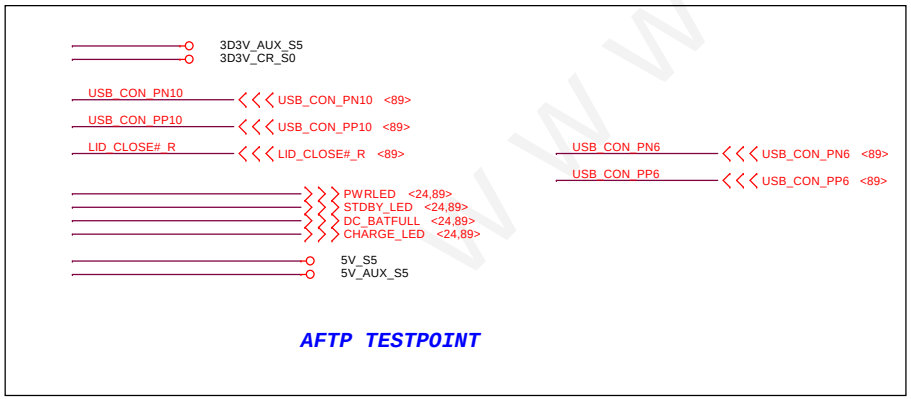
PD 0627 change



PD 0624 change



LAB2 0401 change



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Title
Hall Sensor(Reserved)

Size	Document Number	Rev
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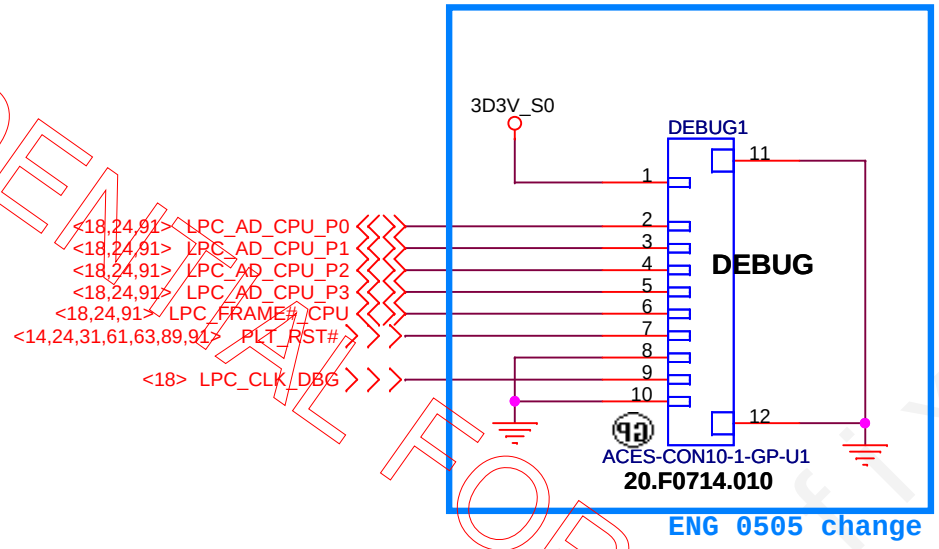

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Title: ***Debug connector***

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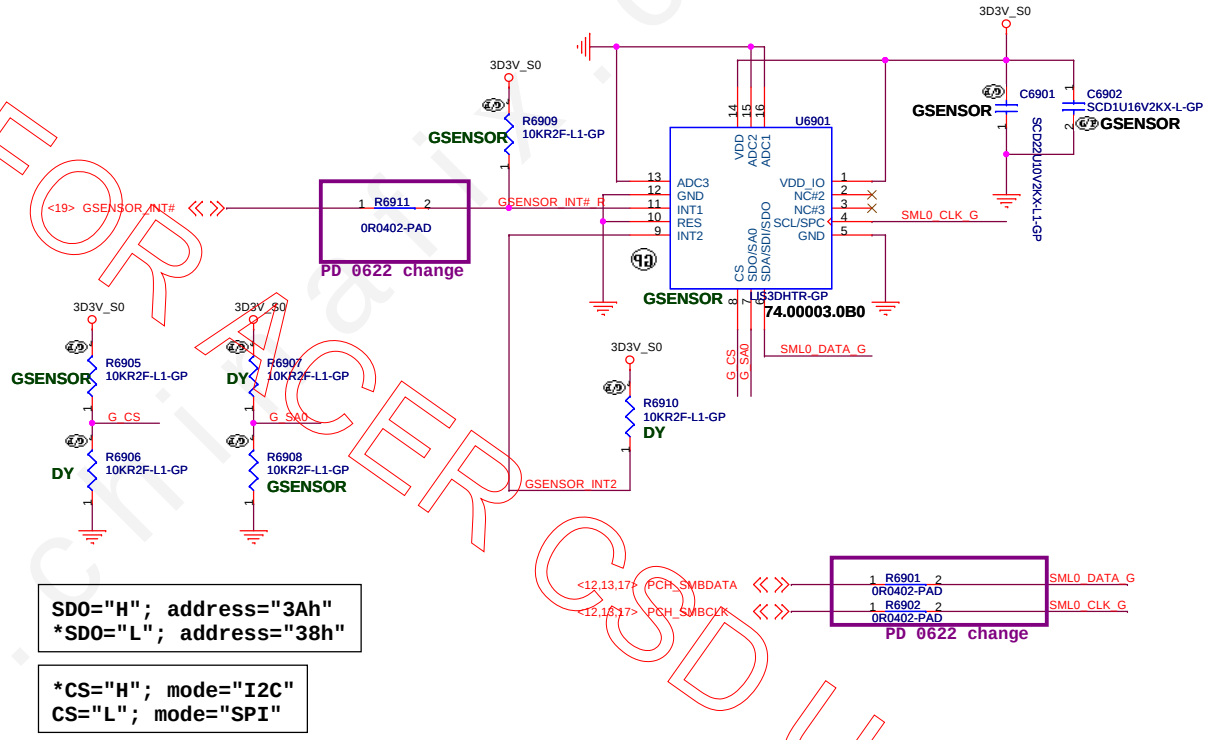
SSID = User.Interface

G Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

CHECK WITH MICK



SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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Title: G-SENSOR

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Title
(Reserved)Free Fall Sensor

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Title: (Reserved)Thunderbolt

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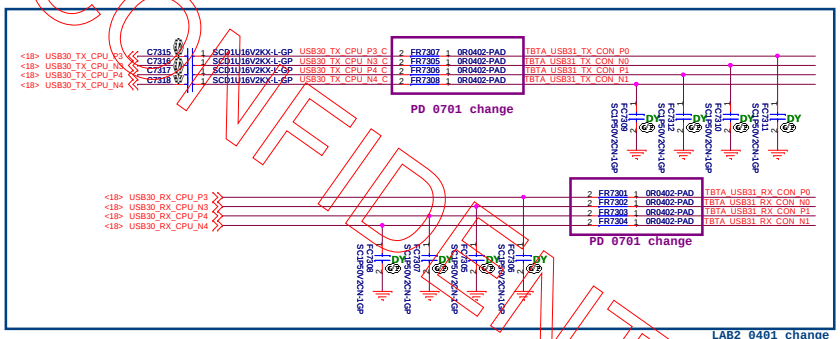

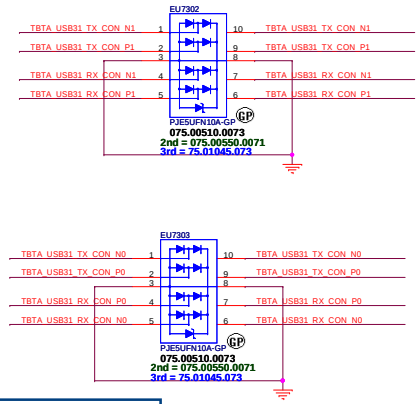

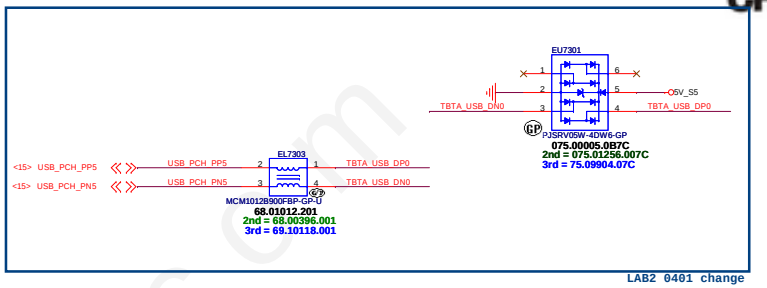

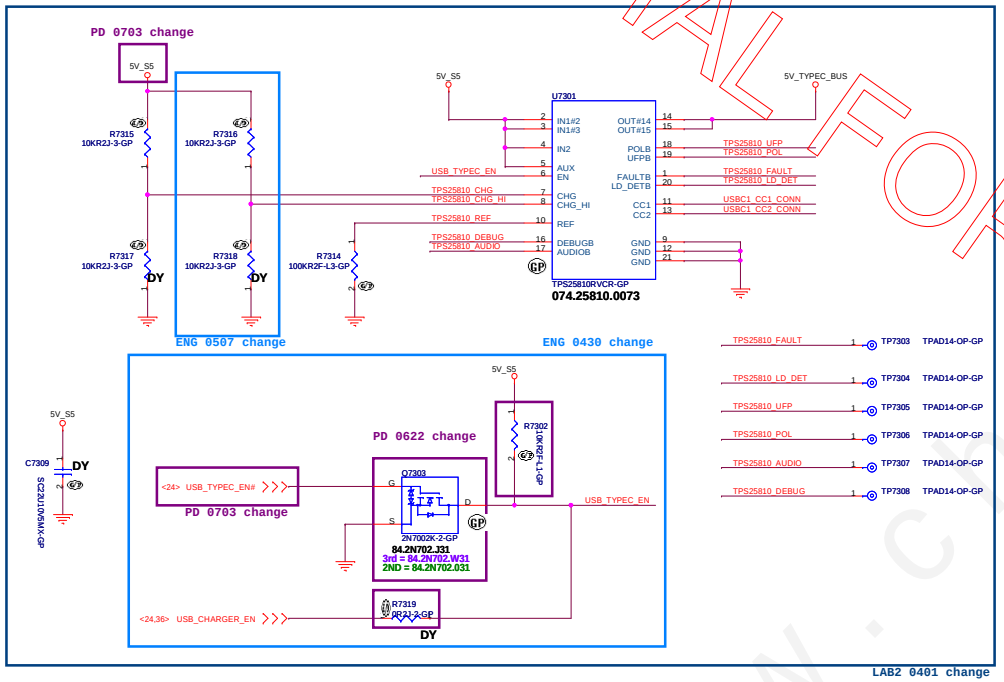

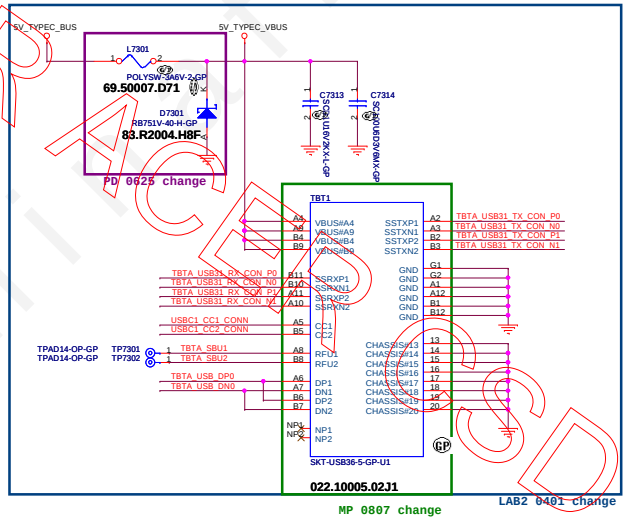

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

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Title: Thunderbolt

Size: A2 | Document Number: Newgate | Rev: 1M

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Title

(Reserved)Thunderbolt (4/5)

Size	Document Number	Rev
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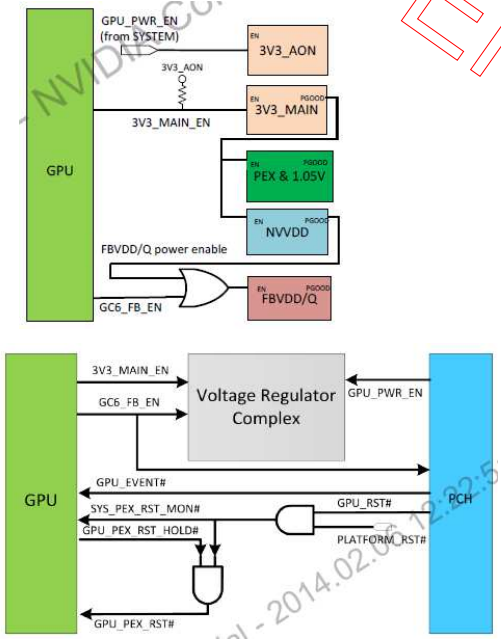
Title: ***(Reserved)Thunderbolt (5/5)***

Size	Document Number	Rev
A	**Newgate**	**1M**

Date: Wednesday, August 12, 2015 Sheet 75 of 105



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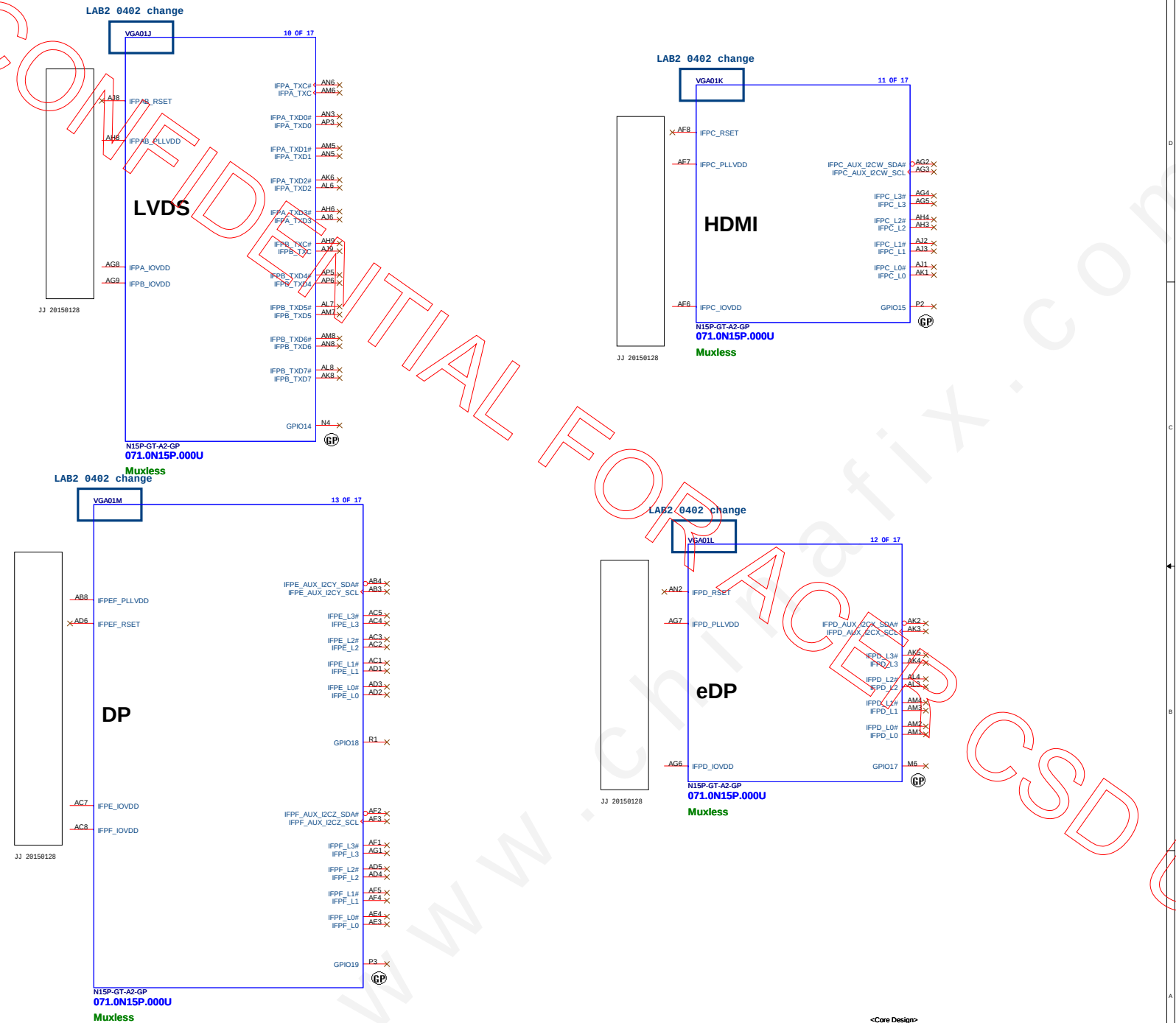

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Title: GPU_DIGITALOUT (2/5)

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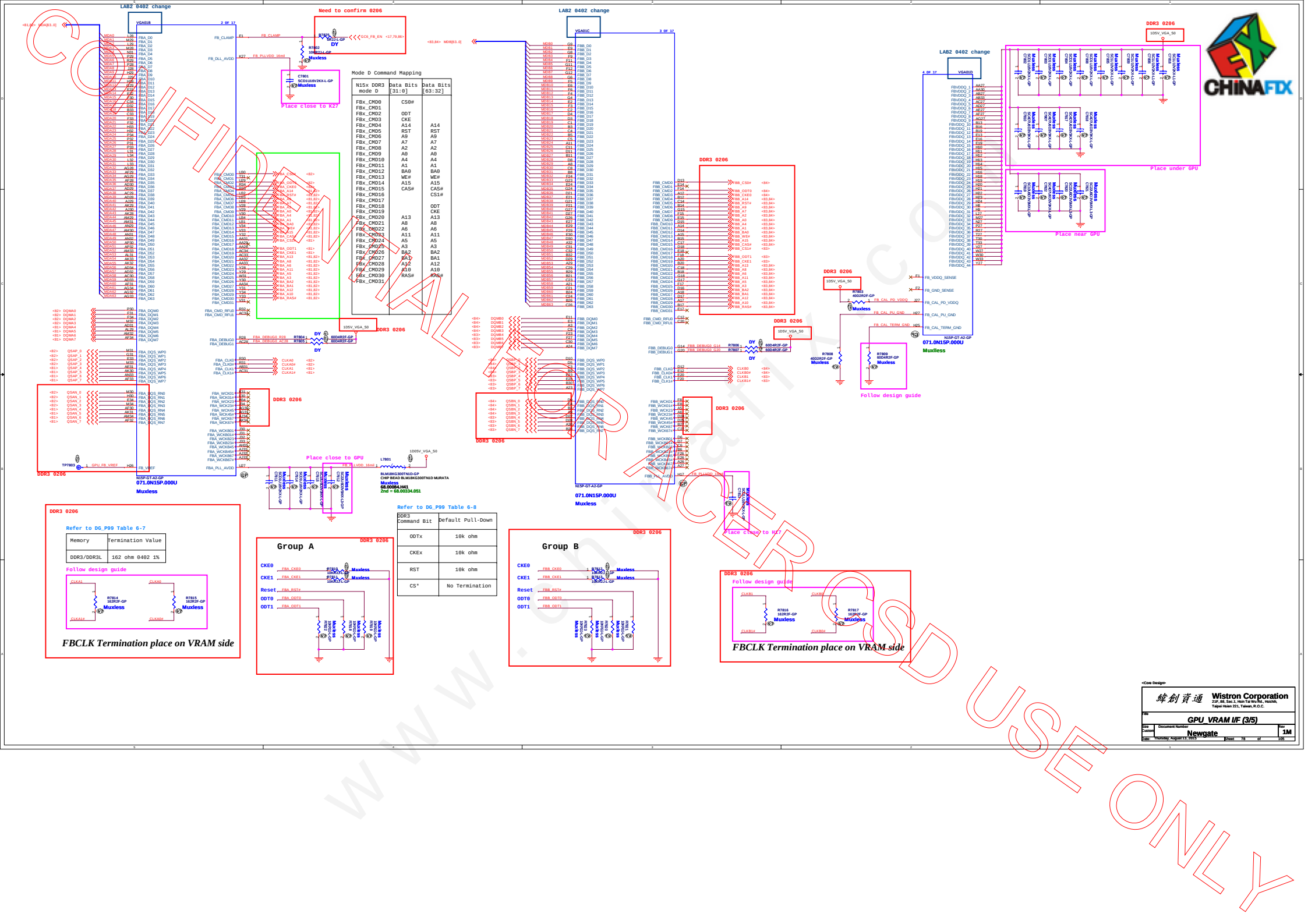
Date: Thursday, August 13, 2015 Sheet 77 of 105


LAB2 0402 change
Need to confirm 0206
DDR3 0206
Mode D Command Mapping
N15x DDR3 mode D
Data Bits [31:0]
Data Bits [63:32]
FBx_CMD0 CS0#
FBx_CMD1 ODT
FBx_CMD2 CKE
FBx_CMD3 A14 A14
FBx_CMD4 RST RST
FBx_CMD5 A9 A9
FBx_CMD6 A7 A7
FBx_CMD7 A2 A2
FBx_CMD8 A0 A0
FBx_CMD9 A4 A4
FBx_CMD10 A1 A1
FBx_CMD11 BA0 BA0
FBx_CMD12 WE# WE#
FBx_CMD13 A15 A15
FBx_CMD14 CAS# CAS#
FBx_CMD15 CS1#
FBx_CMD16
FBx_CMD17 ODT
FBx_CMD18 CKE
FBx_CMD19 A13 A13
FBx_CMD20 A8 A8
FBx_CMD21 A6 A6
FBx_CMD22 A11 A11
FBx_CMD23 A5 A5
FBx_CMD24 A3 A3
FBx_CMD25 BA2 BA2
FBx_CMD26 BA1 BA1
FBx_CMD27 A12 A12
FBx_CMD28 A10 A10
FBx_CMD29 RAS# RAS#
FBx_CMD30
FBx_CMD31
Place close to K27
Place close to GPU
Place close to K17
Place under GPU
Place near GPU
Follow design guide
071.0N15P.000U
Muxless
Refer to DG_P99 Table 6-7
Memory
Termination Value
DDR3/DDR3L
162 ohm 0402 1%
Refer to DG_P99 Table 6-8
DDR3 Command Bit
Default Pull-Down
ODTx
10k ohm
CKEx
10k ohm
RST
10k ohm
CS*
No Termination
Group A
Group B
FBCLK Termination place on VRAM side
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GPU_VRAM I/F (3/5)
Newgate
1M
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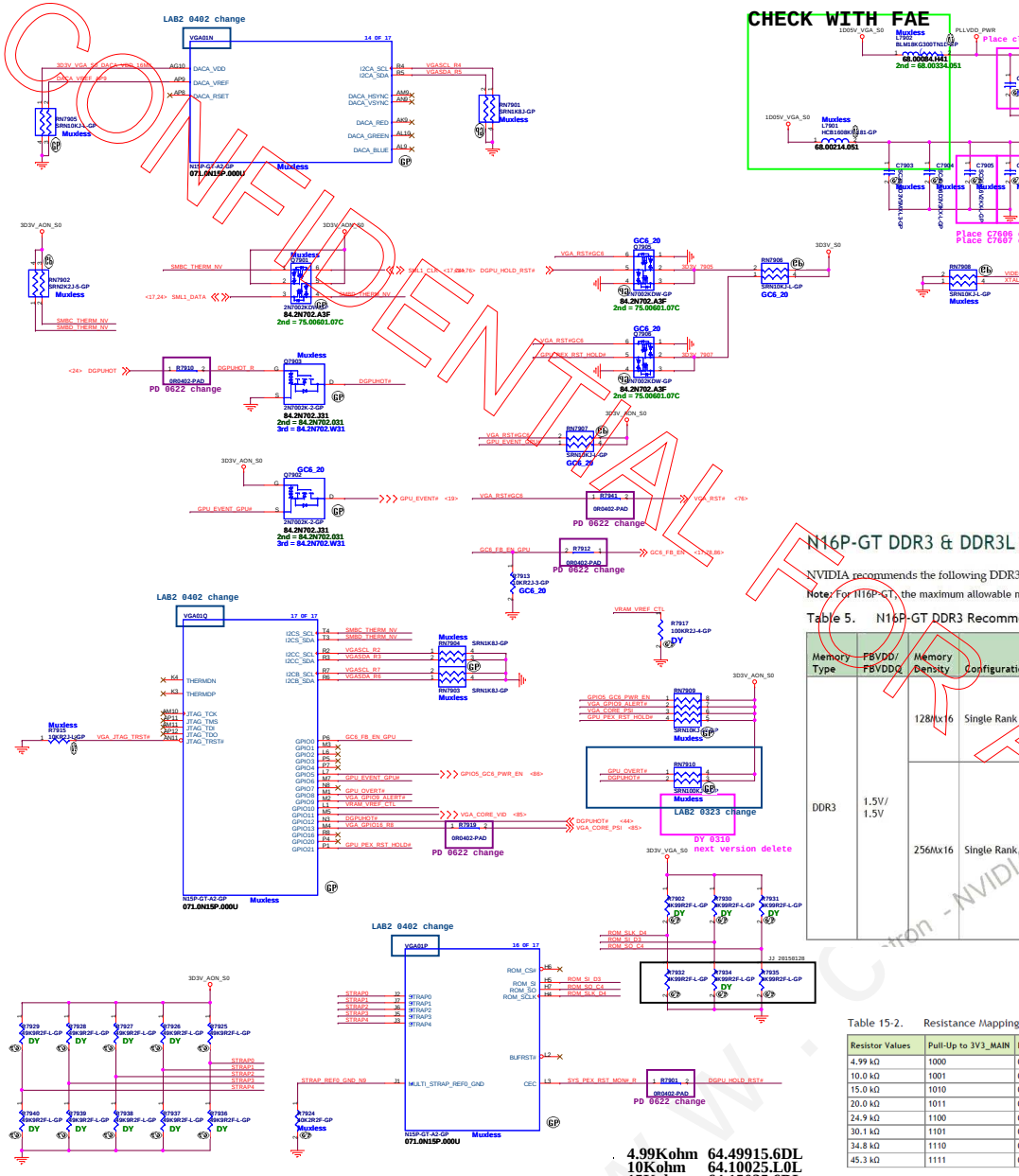

N16P-GT DDR3 & DDR3L MEMORY RVL

NVIDIA recommends the following DDR3 and DDR3L memories for use in conjunction with notebook designs using N16P-GT.

Note: For N16P-GT, the maximum allowable memory case temperature is 85 °C.

Table 5. N16P-GT DDR3 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Configuration	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
DDR3	1.5V/ 1.5V	128Mx16	Single Rank	Hynix	H5TC2G63FFR-11C	F-die	0x6	1000	N/A	Production ready
				Micron	MT41J128M16JT-093G:K	K-die	0x7	1000	1322	Production ready
				Samsung	K4W2G1646Q-BC1A	Q-die	0x8	1000	N/A	Production ready
		256Mx16	Single Rank	Hynix	H5TC4G63AFR-11C	A-die	0x0	1000	N/A	Production ready
				Micron	MT41J256M16HA-093G:E	E-die	0x1	1000	1322	Production ready
				Samsung	K4W4G1646D-BC1A	D-die	0x2	1000	N/A	Production ready
				Samsung	K4W4G1646E-BC1A	E-die	0x4	1000	N/A	Post production ready
				Hynix	H5TC4G63CFR-H0C	C-die	0x5	1000	N/A	Post production ready

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			

4.99Kohm 64.49915.6DL
10Kohm 64.10025.L0L
15Kohm 64.15025.6DL
20Kohm 64.20025.6DL
24.9Kohm 64.24925.6DL
30.1Kohm 64.30125.6DL
34.8Kohm 64.34825.6DL
45Kohm 64.45325.6DL

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GPU_GPIO/STRAP
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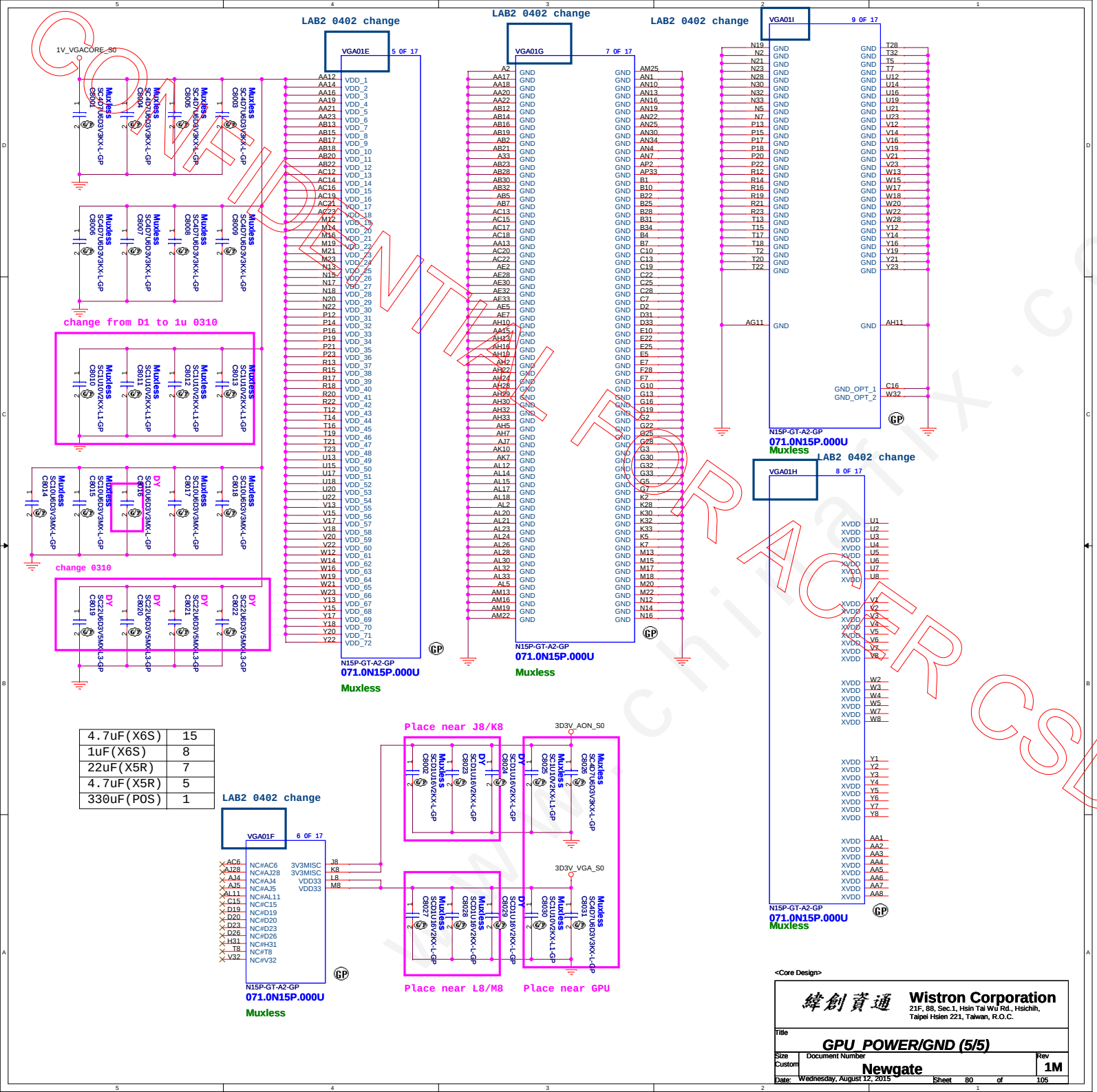

4.7uF(X6S)	15
1uF(X6S)	8
22uF(X5R)	7
4.7uF(X5R)	5
330uF(POS)	1

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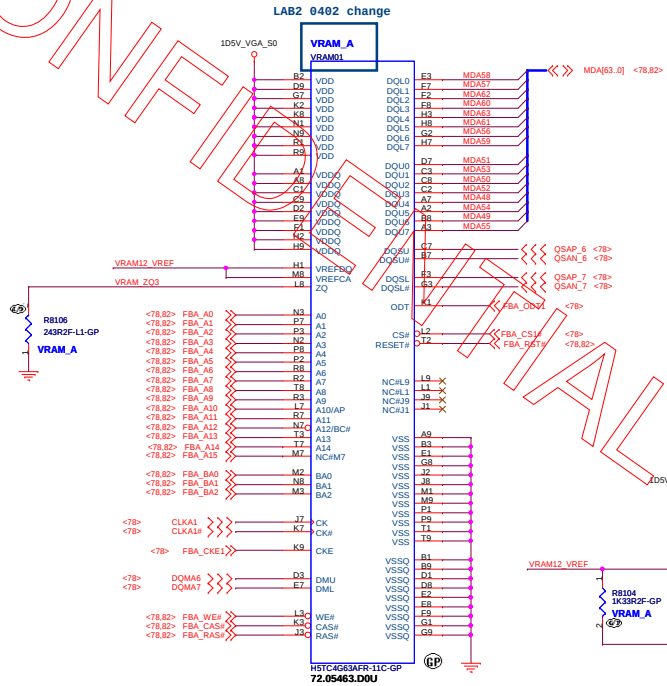
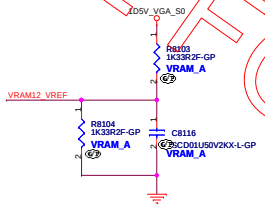
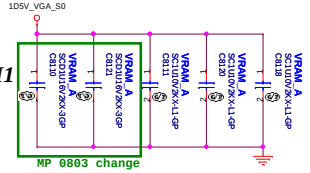
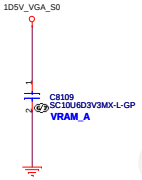






FOR VRAM1



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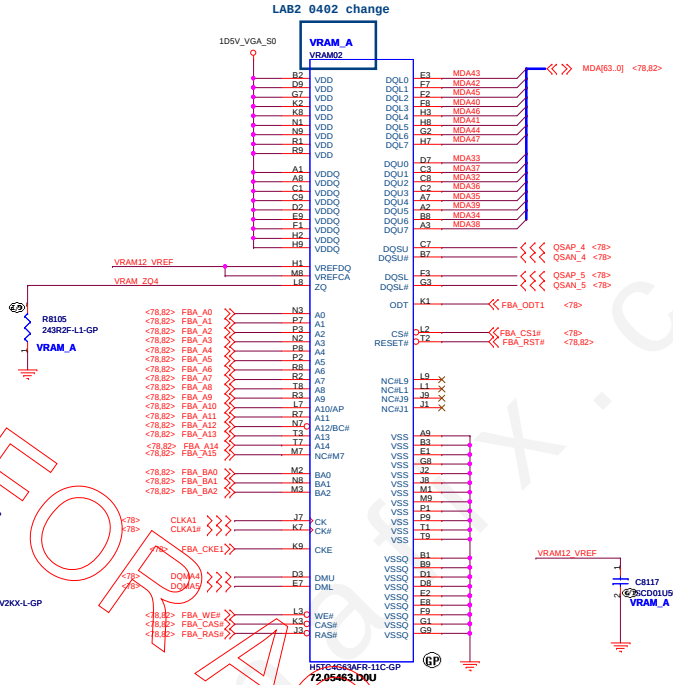

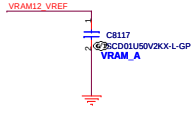

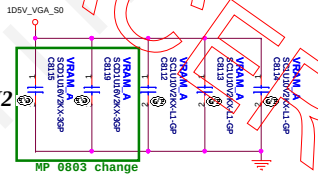

FOR VRAM2

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Title	VRAM CHANNEL_A_1&2	
Size: A2	Document Number: Newgate	Rev: 1M
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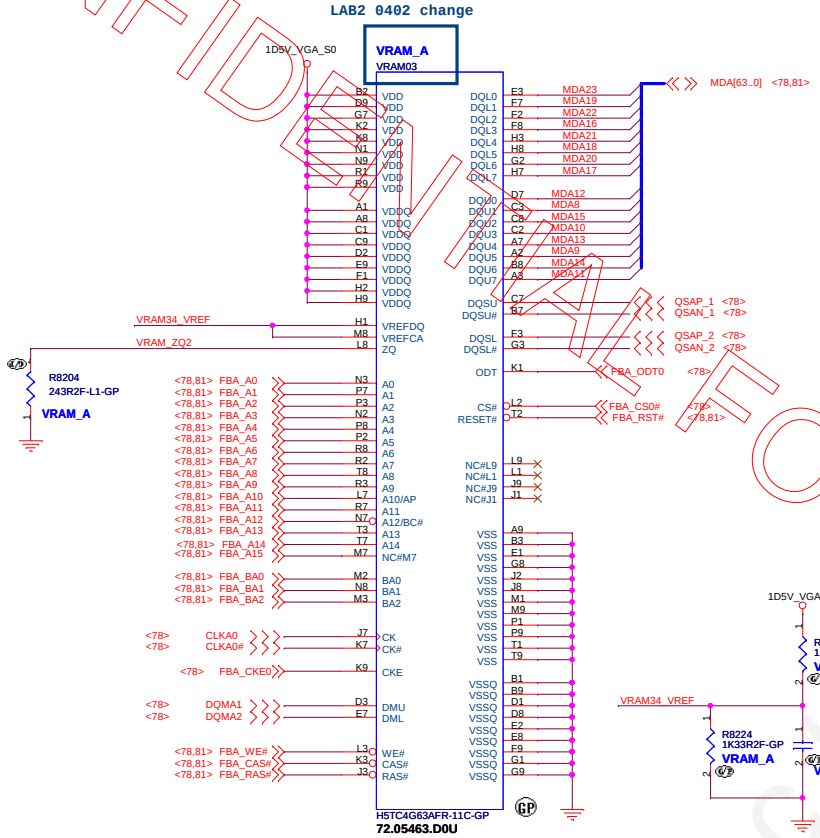

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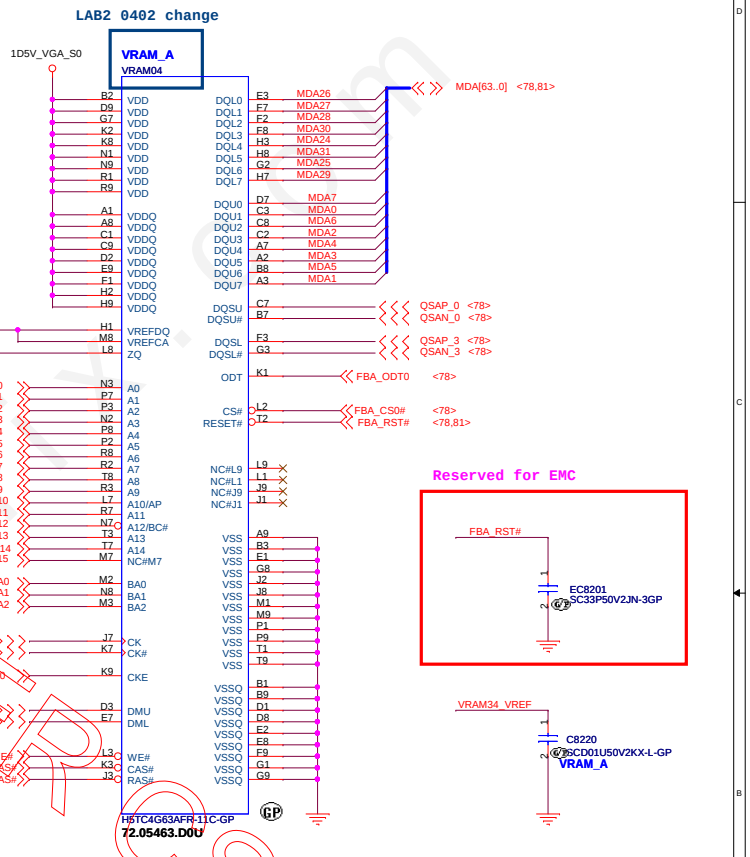
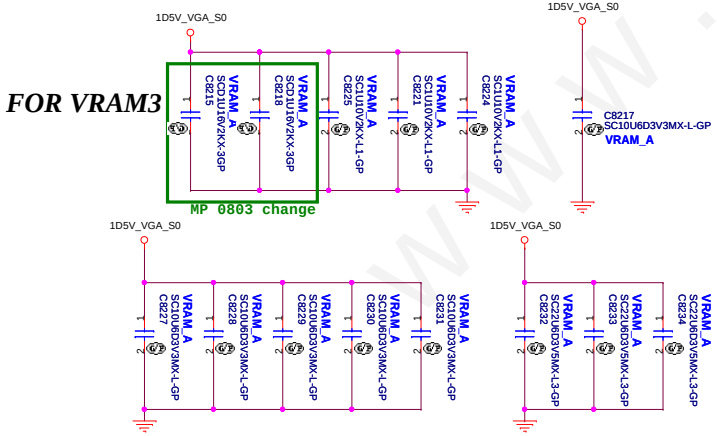
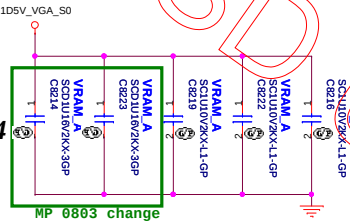


FOR VRAM3



FOR VRAM4



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Title: VRAM CHANNEL_A_3&4

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LAB2 0402 change

VRAM_B
VRAM05

1D5V_VGA_S0

H5TC4G63AFR-11C-GP
72.05463.D0U

R8301 243R2F-L1-GP VRAM_B

VRAM56_VREF
VRAM_ZQ7

1D5V_VGA_S0

R8302 1K33R2F-GP VRAM_B
R8303 1K33R2F-GP VRAM_B
C8318 SCD01U50V2KX-L-GP VRAM_B

LAB2 0402 change

VRAM_B
VRAM06

1D5V_VGA_S0

H5TC4G63AFR-11C-GP
72.05463.D0U

R8304 243R2F-L1-GP VRAM_B

VRAM56_VREF
VRAM_ZQ8

C8317 SCD01U50V2KX-L-GP VRAM_B

FOR VRAM5

1D5V_VGA_S0

C8801 SC10U16V2KX-3GP VRAM_B
C8802 SC10U16V2KX-3GP VRAM_B
C8803 SC10U10V2KX-L-GP VRAM_B
C8804 SC10U10V2KX-L-GP VRAM_B
SC10U10V2KX-L-GP VRAM_B

MP 0803 change

FOR VRAM6

1D5V_VGA_S0

C8309 SC10U6D3V3MX-L-GP VRAM_B

1D5V_VGA_S0

C8310 SC10U16V2KX-3GP VRAM_B
C8311 SC10U16V2KX-3GP VRAM_B
C8312 SC10U10V2KX-L-GP VRAM_B
C8313 SC10U10V2KX-L-GP VRAM_B
C8314 SC10U10V2KX-L-GP VRAM_B

MP 0803 change

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Title: VRAM CHANNEL_B_5&6

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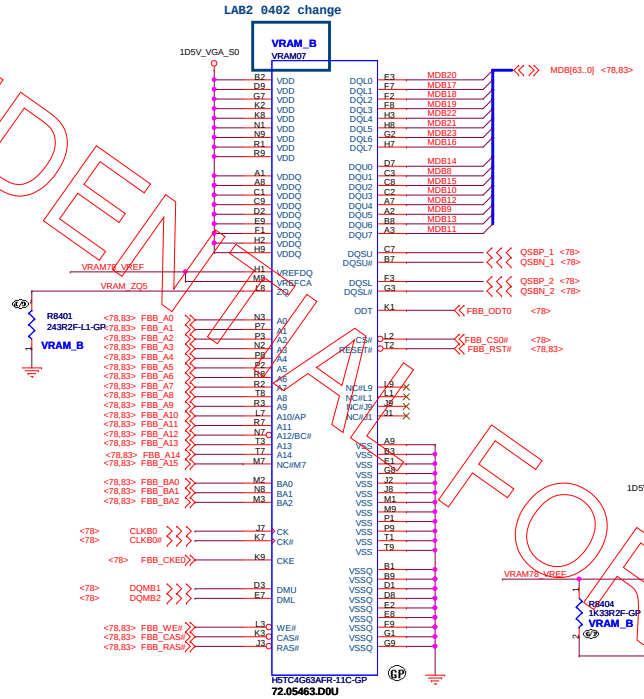

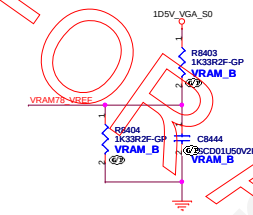

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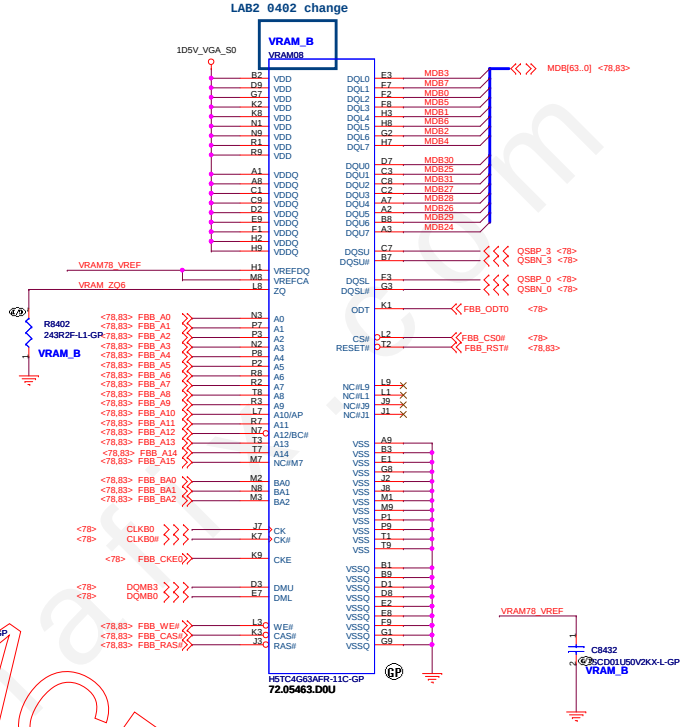
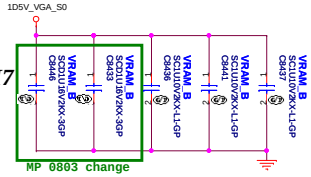
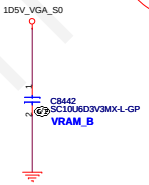
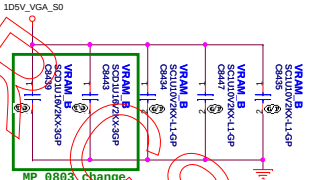


FOR VRAM7





FOR VRAM8



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VGA : N15P GX
Config : B
EDP-Continuous : 49A
EDP-Peak : 76A

CHECK SPEC

	Config : D	Config : C	Config : B
EDP-Cont.	33.5 A	35 A	43 A
EDP-Peak	51.5 A	40.89 A	80 A
PR8222	27K ohm	39K ohm	20K ohm
PR8206	7.5K ohm	30K ohm	20K ohm
PR8208	0 ohm	3K ohm	2K ohm
PR8209	6.2K ohm	24K ohm	18K ohm
PR8214	1.74K ohm	3K ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF

79.15612.03L
PD 0626 change

CHECK WITH WAYLER MORRIS

請wayler SHOT PAD 都改回0 ohm

Poisent(13.3k) and hades setting different!!??

OCP setting

RT8813AGQW-GP

RT9610BZQW-GP

FDMS3600-02-RJK0215-COLAY-GP
1st = 84.00916.037
2nd = 84.03660.037
Muxless

Mag. 0.36uH 7*7*4
DCR=1.8~2.3mohm
Idc=23A, Isat=32A

470uF/2V, 7.5 x 4.5 x 2.1
ESR=9mohm
Ripple Current=3000 mA

ENG 0527 change

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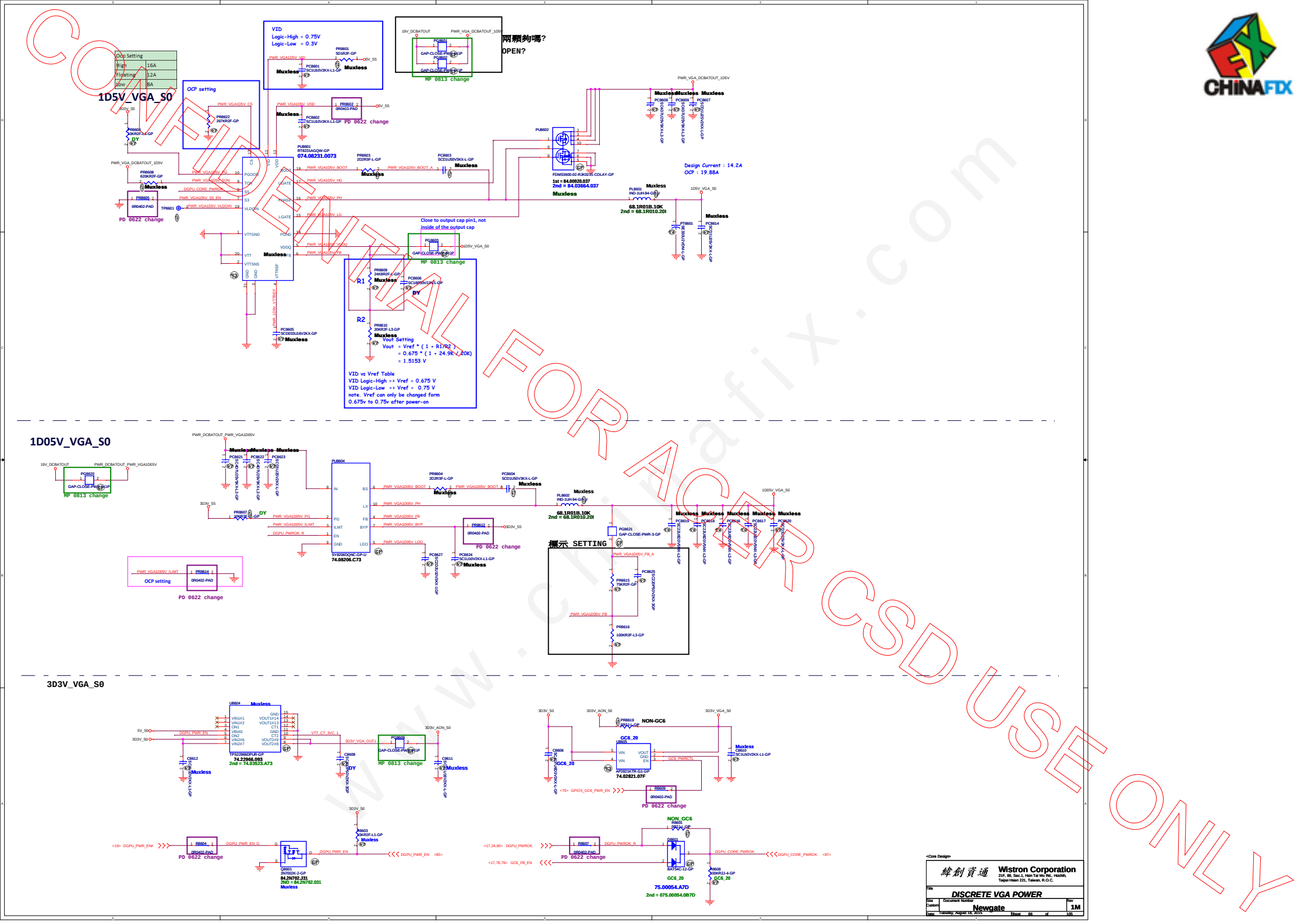

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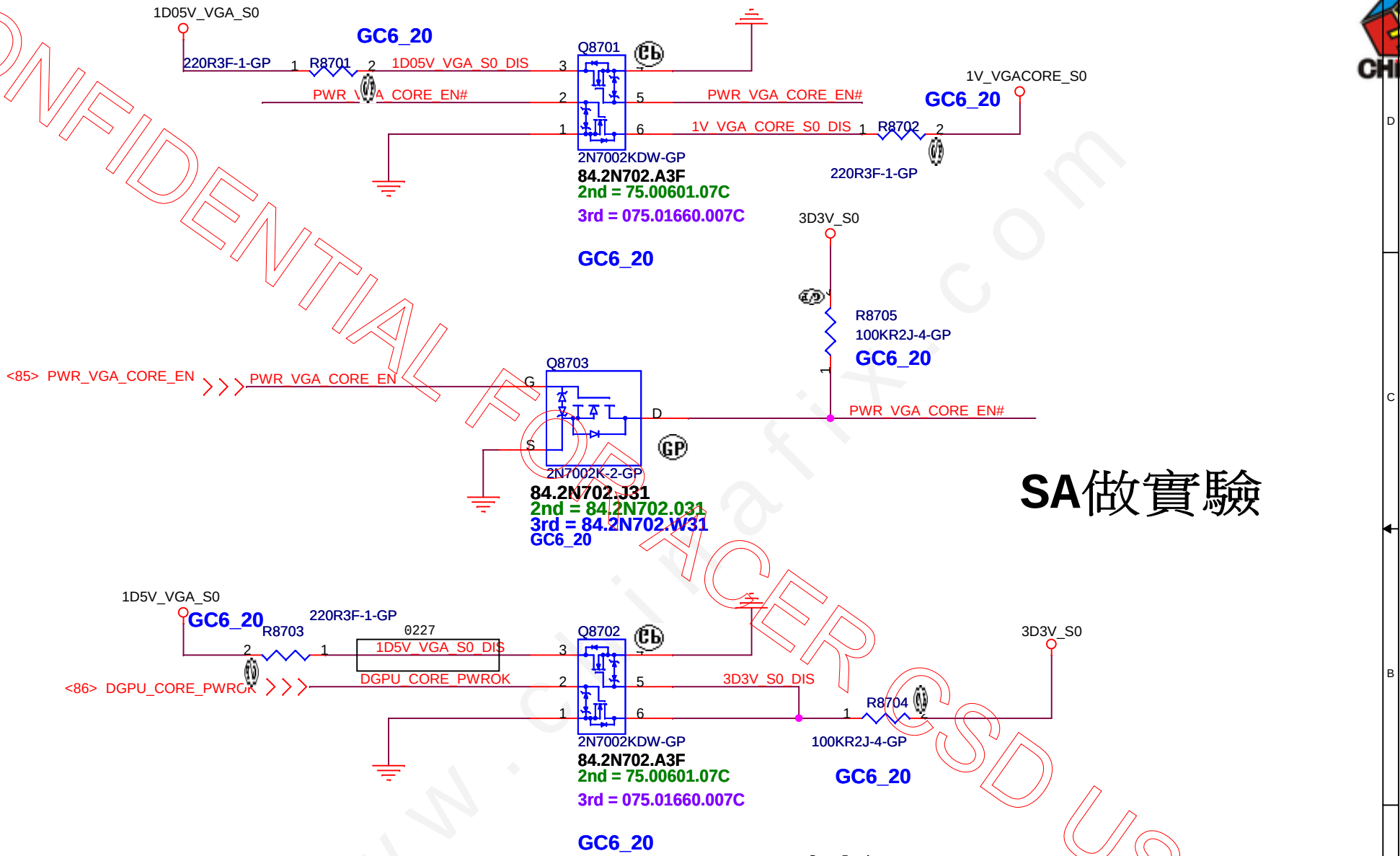

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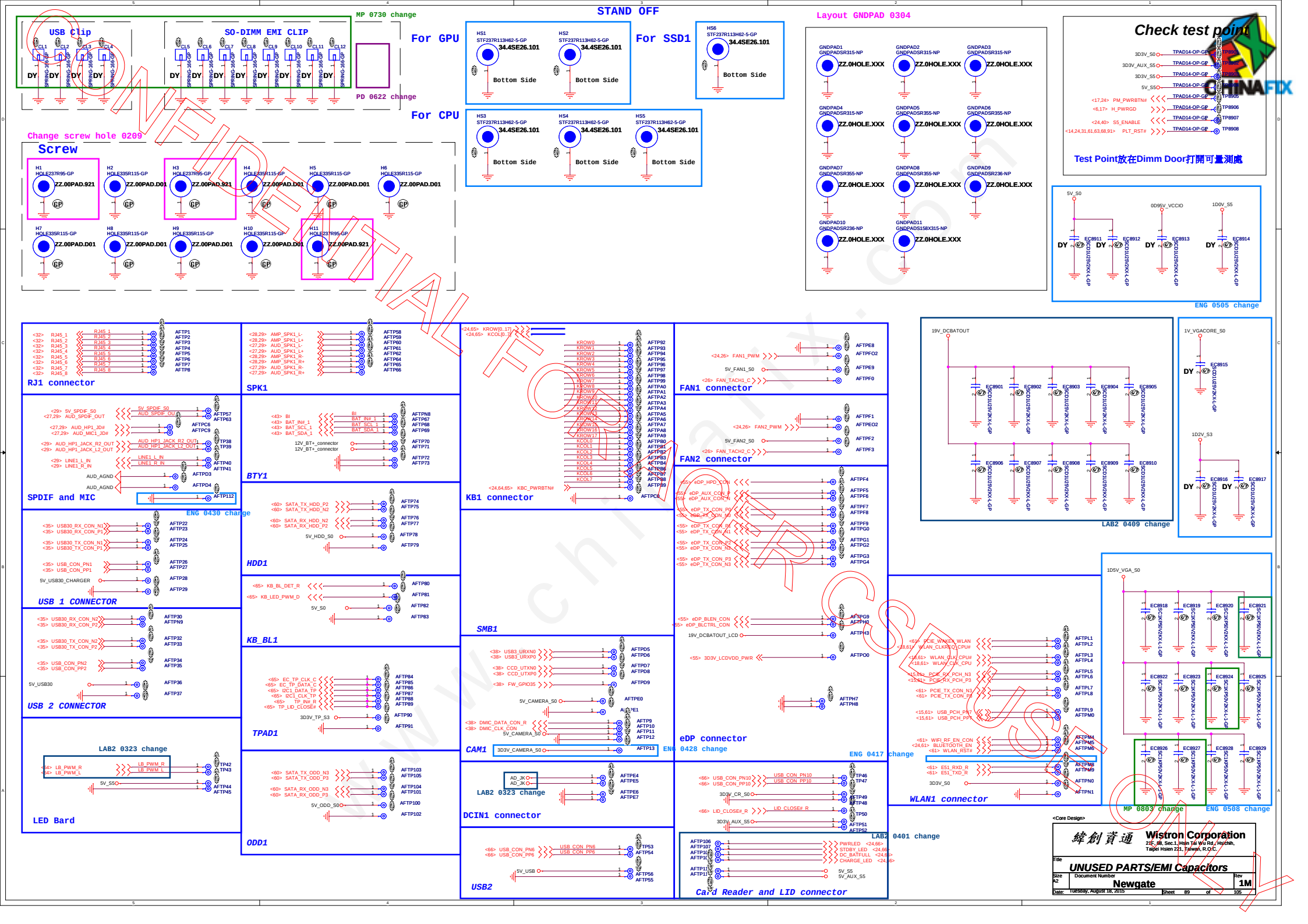
USB Clip
SO-DIMM EMI CLIP
MP 0730 change
PD 0622 change
For GPU
For SSD1
For CPU
STAND OFF
Layout GNDPAD 0304
Check test point
Test Point放在Dimm Door打開可量測處
Change screw hole 0209
Screw
RJ1 connector
SPK1
BTY1
SPDIF and MIC
ENG 0430 change
HDD1
USB 1 CONNECTOR
KB_BL1
USB 2 CONNECTOR
TPAD1
LAB2 0323 change
LED Bard
ODD1
KB1 connector
SMB1
CAM1
ENG 0428 change
DCIN1 connector
LAB2 0323 change
USB2
FAN1 connector
FAN2 connector
eDP connector
ENG 0417 change
Card Reader and LID connector
LAB2 0401 change
LAB2 0409 change
ENG 0505 change
WLAN1 connector
MP 0803 change
ENG 0508 change
ENG 0508 change
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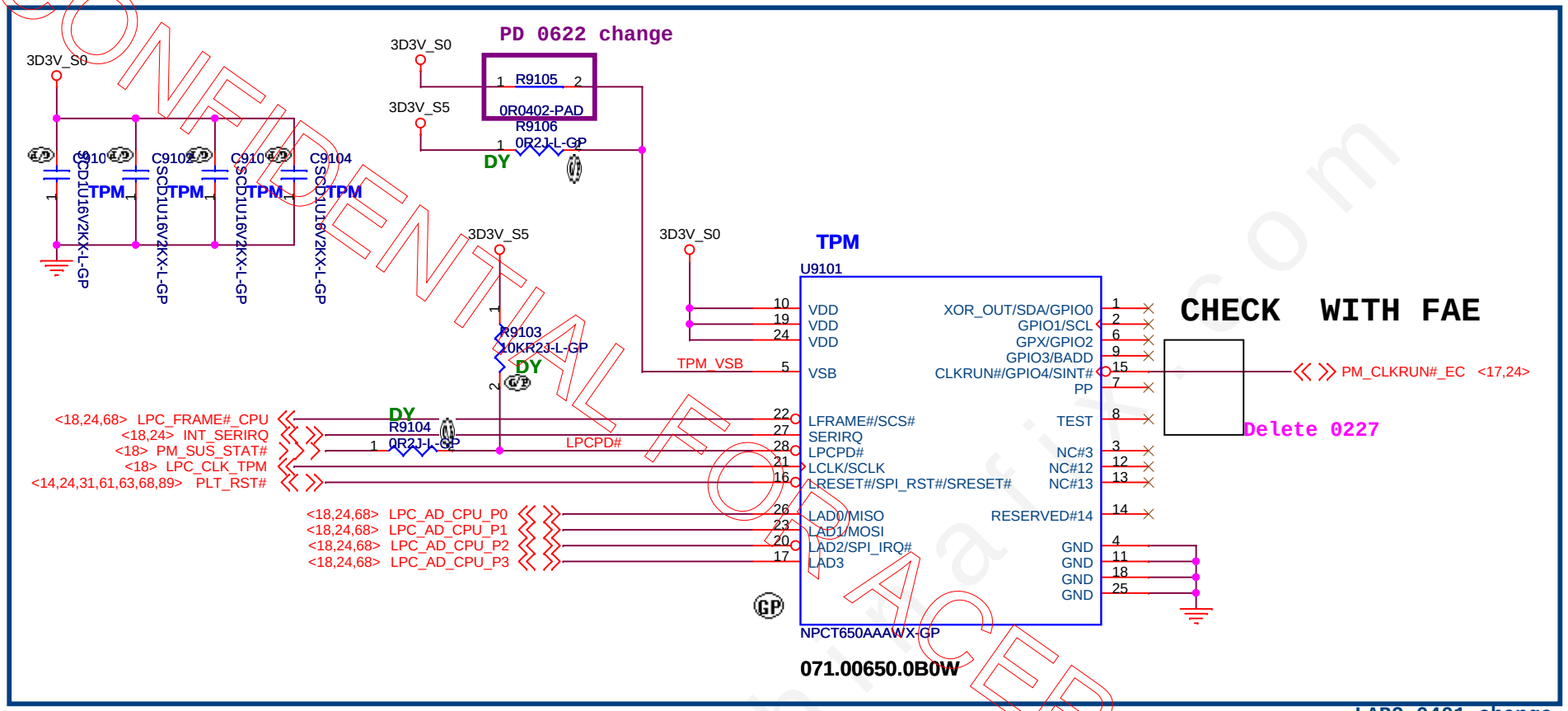

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CPU_CFG_CFG STRAP

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Title: ***CPU_CFG_CFG STRAP***

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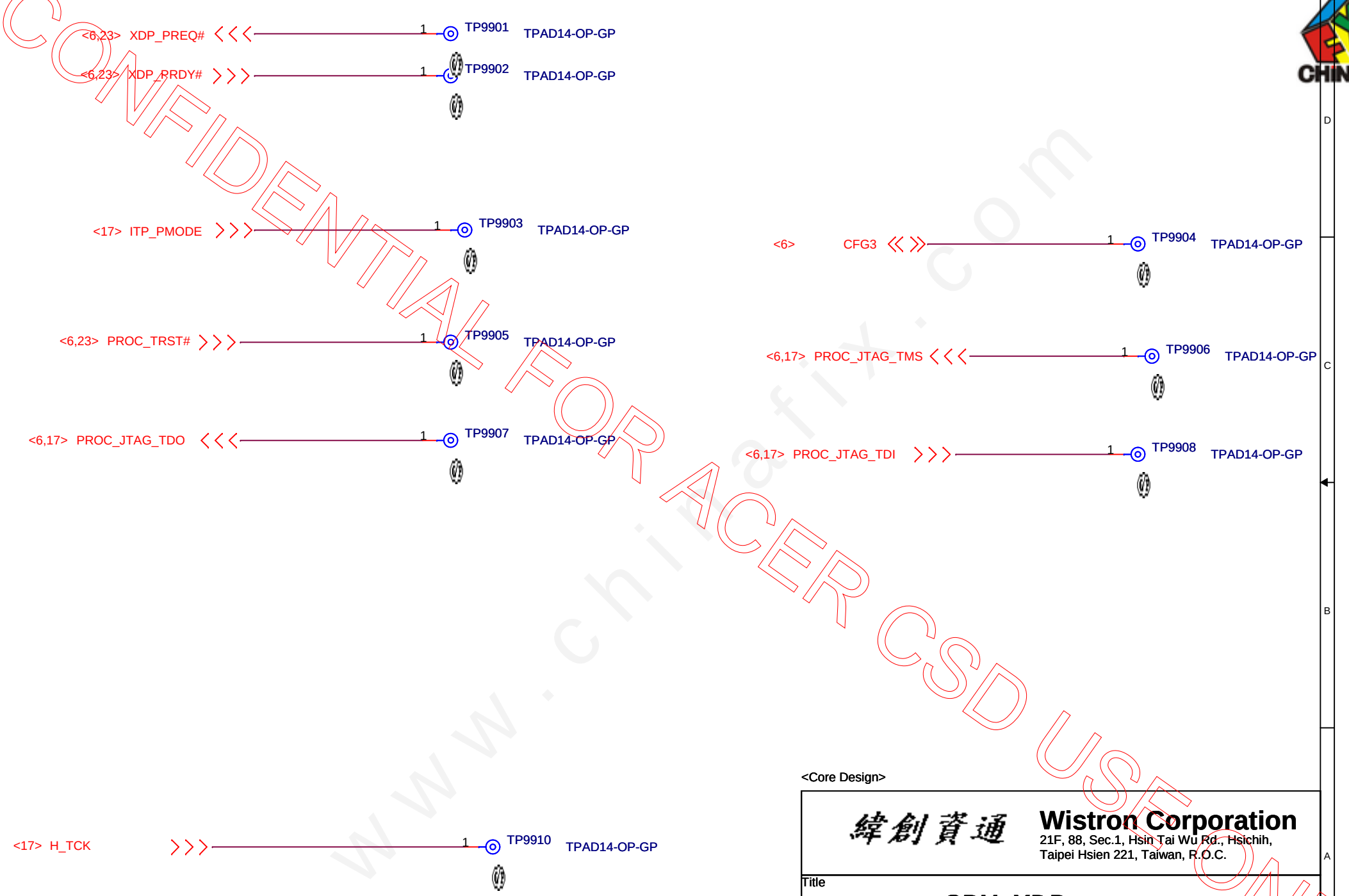

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Intel-Power Up Sequence

(AC mode)

RTC_AUX_S5
RTC_RST#
3D3V_AUX/5V_AUX
ECREST
5V_CHARGER_EN
3V_5V_EN
5V_S5/3D3V_S5
3V_5V_POK
PM_SLP_SUS
3D3V_SUS
RSMRST#
PM_SUSWARN#
AC_PRESENT

(AC mode) (DC mode)

KBC_PWRBTN_EC#
3V_5V_POK
PM_PWRBTN#

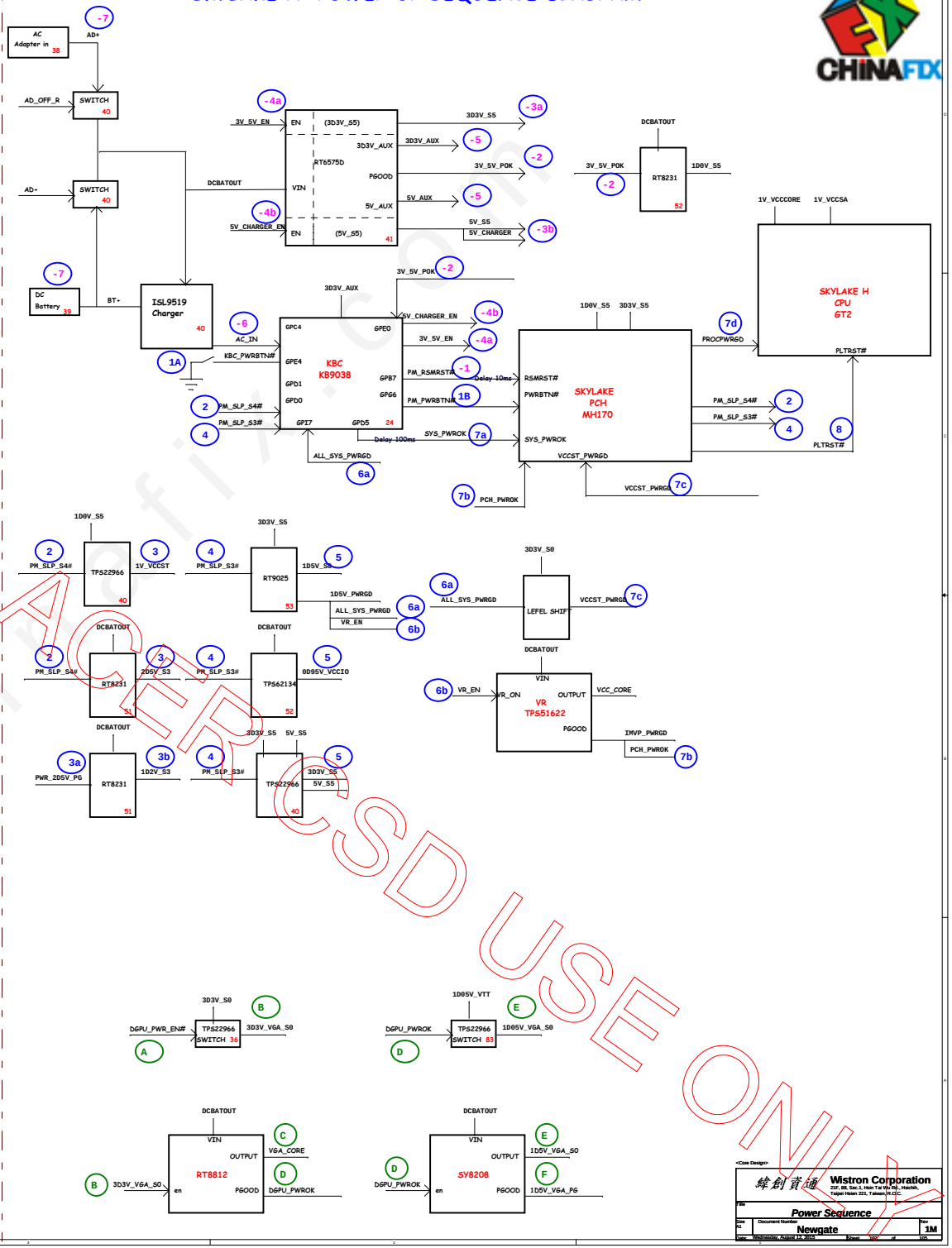
PM_PWRBTN#
PM_SLP_A#
PM_SLP_S4#
1V_VCCST
2D5V_S3
1D25V_S3
PM_SLP_S3#
0D95V_VCCIO
DDR_PG_OUT
0D6V_S0
3D3V_S5/5V_S5
1D5V_S0
ALL_SYS_PWRGD
VR_EN
VCCST_PWRGD
VCC_CORE
IMVP_PWRGD
PROCPWRGD
PLTRST#

DGPU_PWR_EN#(Discrete only)
3D3V_VGA_S0(Discrete only)
VGA_CORE(Discrete only)
DGPU_PWROK(Discrete only)
1D5V_VGA_S0(Discrete only)
1D05V_VGA_S0(Discrete only)

1.05VTT_PWRGD
ALL_SYSTEM_PWRGD
H_VR_EN
+VCC_CORE
<3ms
CPU CORE Power
CLK_CPU_BCLK
CLKIN_BCLK Stable
IMVP_PWRGD
PCH_PWROK

H_CPUPWRGD
ALL_SYSTEM_PWRGD
To KBC GPI7 delay 99ms to PCH
SYS_PWRGD
PLT_RST#

SKYLAKE H POWER UP SEQUENCE DIAGRAM



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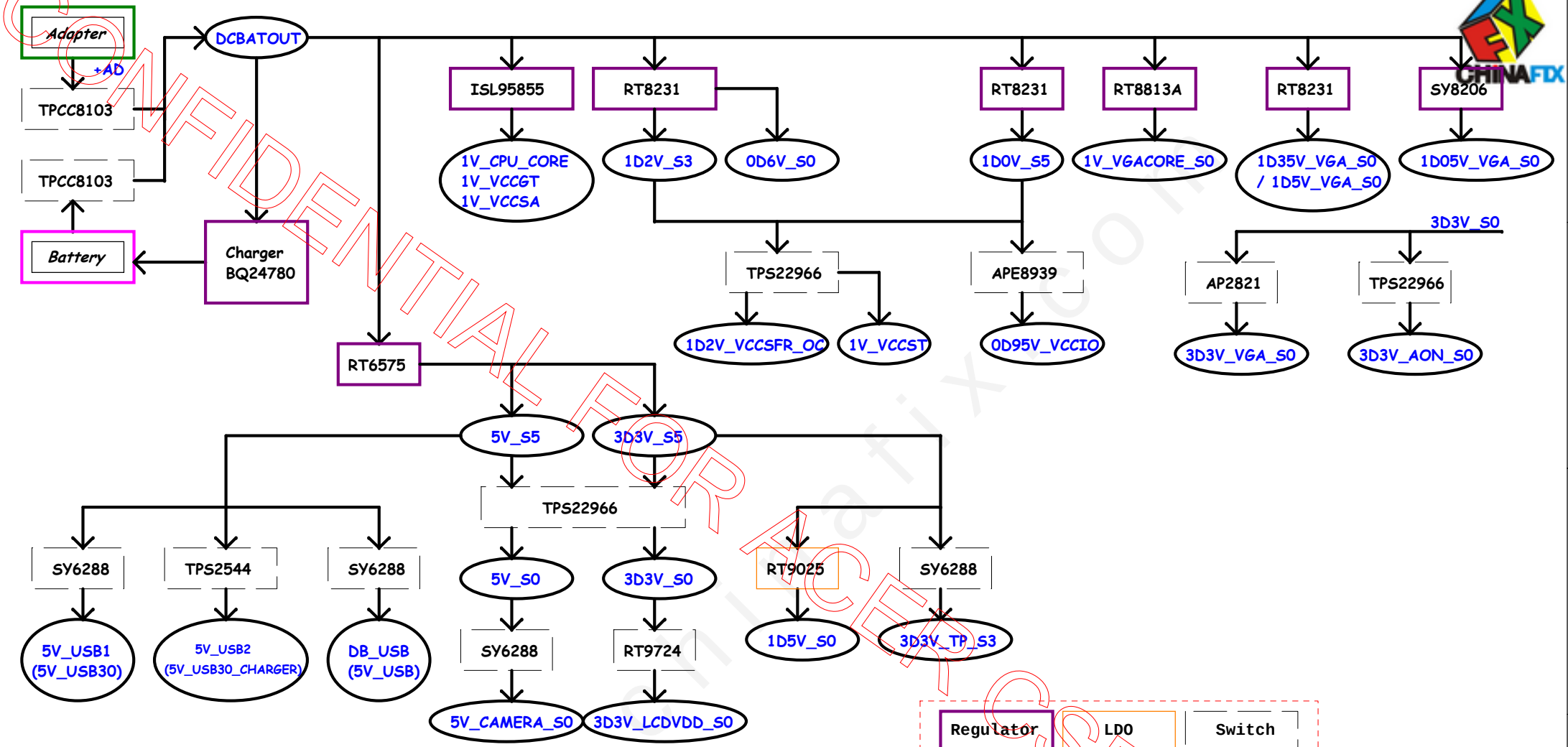

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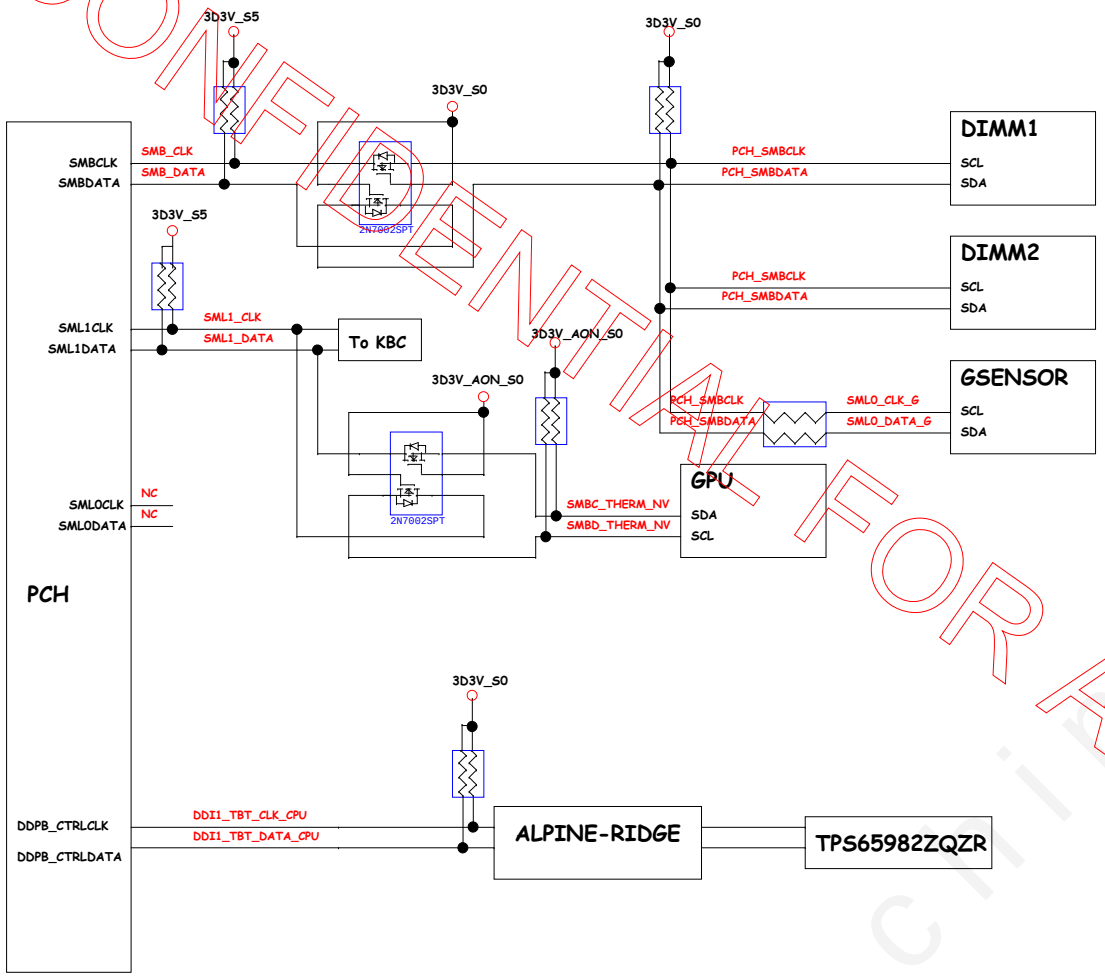
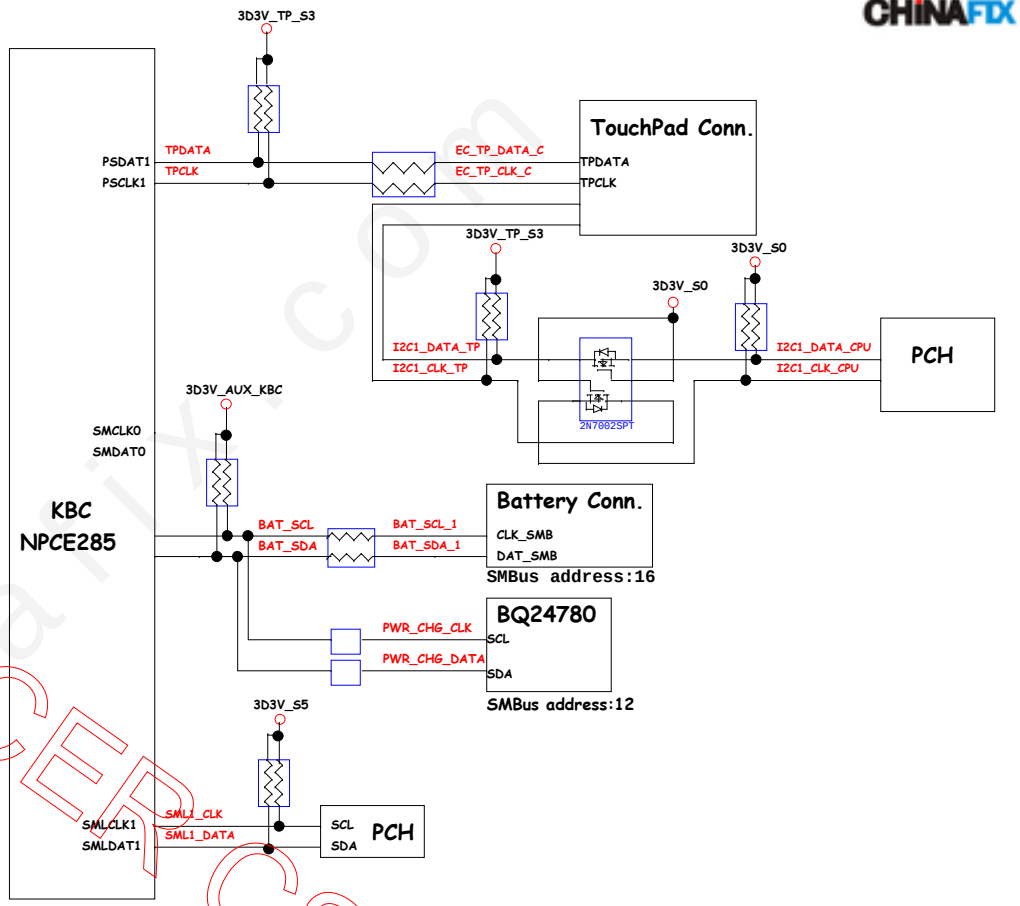
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS BLOCK DIAGRAM

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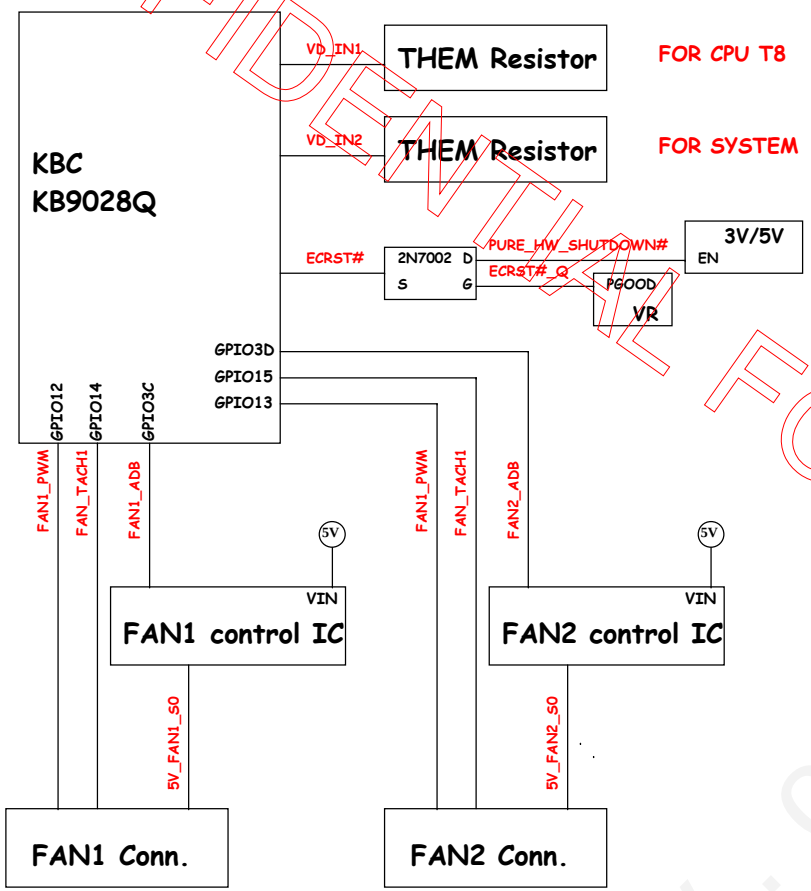
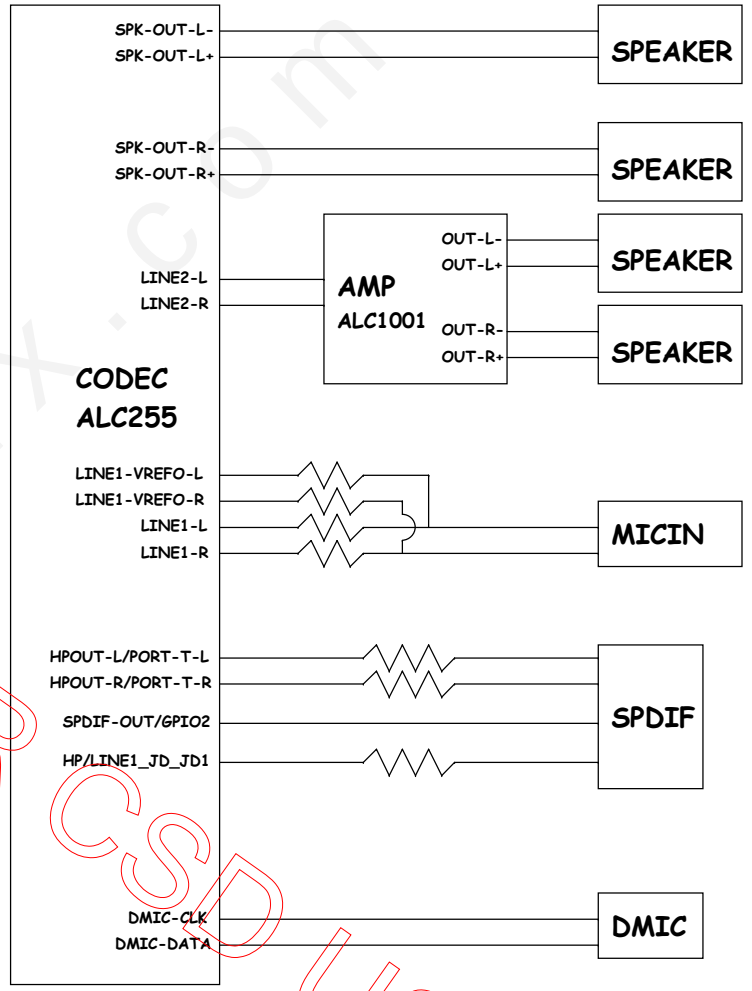
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal /AUDIO Block Diagram

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